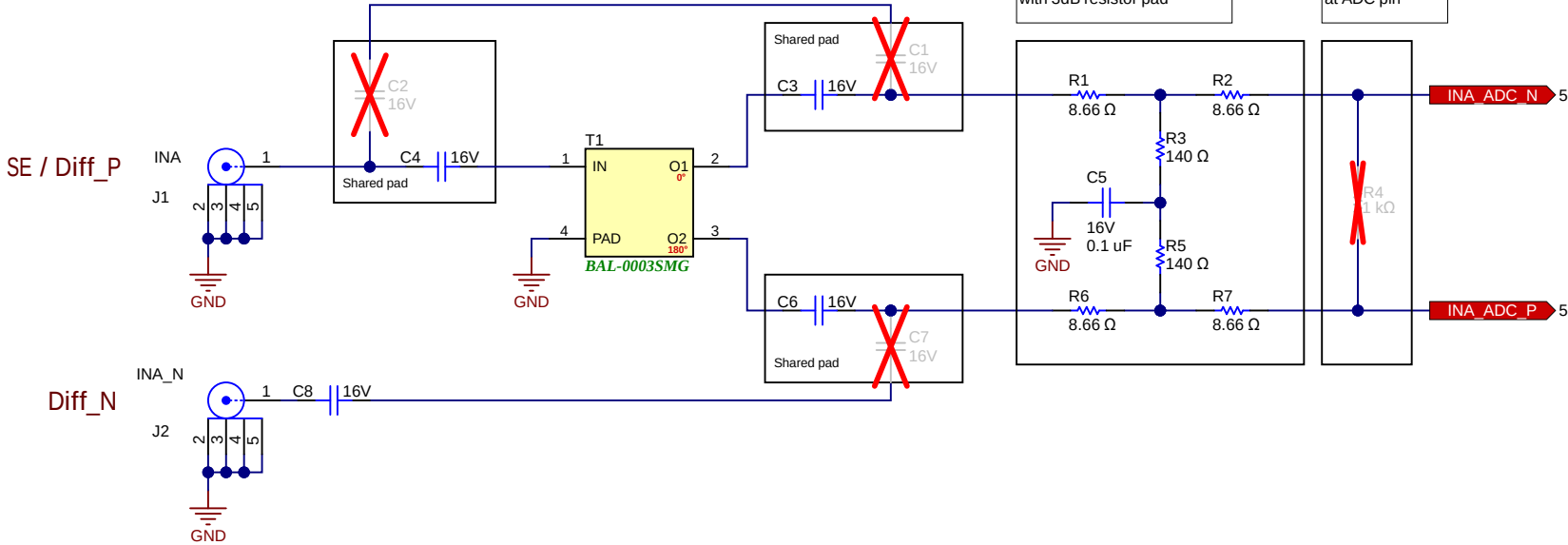


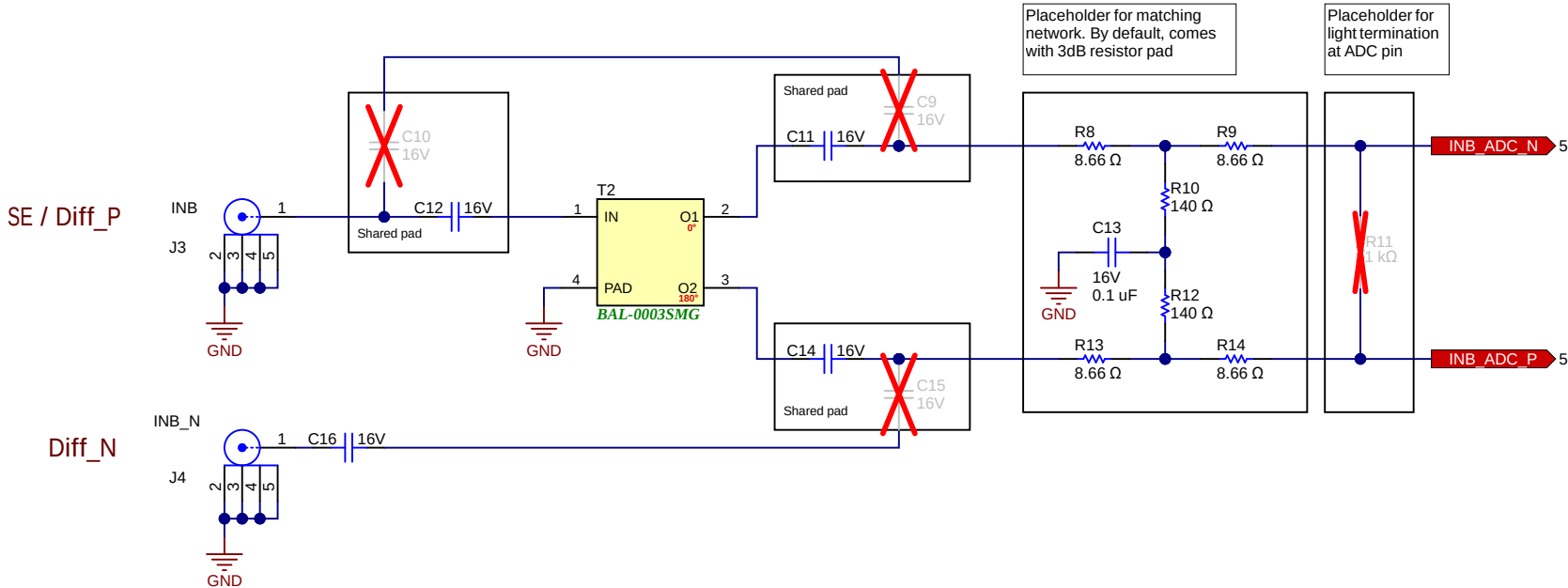
1	2	3	4	5	6	
Block Diagram						
A						A
B						B
C						C
D						D
		Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.				
1	2	3	4	5	6	

ADC EVM RF Input

Channel A

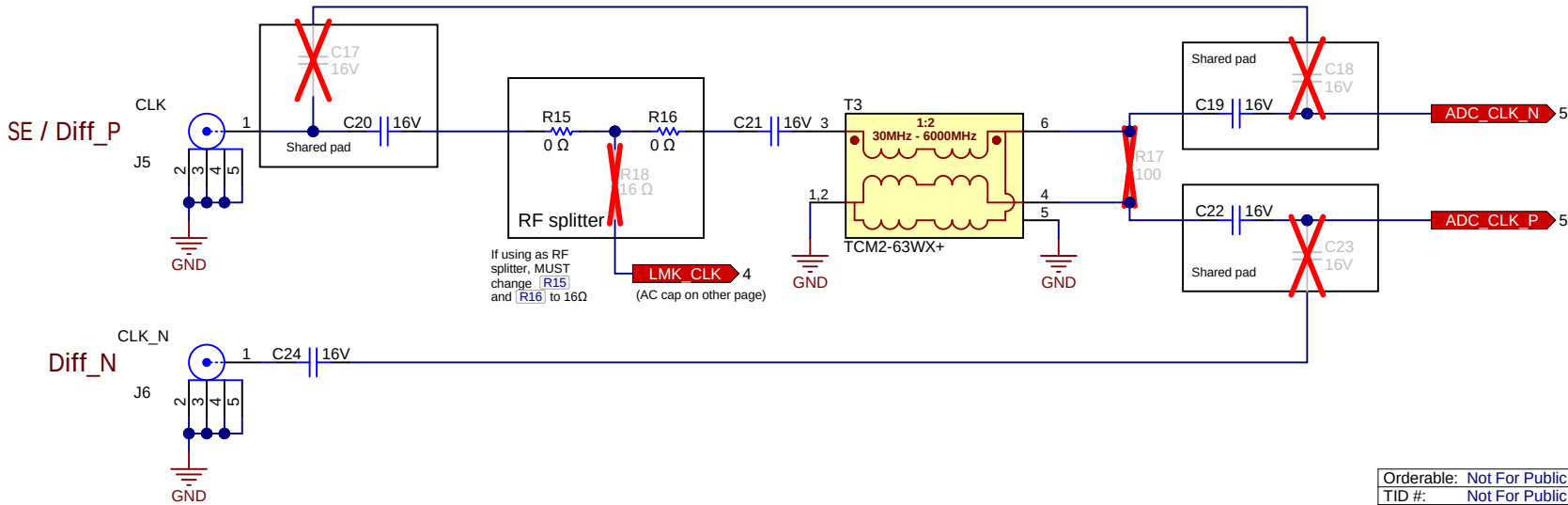


Channel B



Clock input

Differential by default
Note: LMK requires reference clock on input [J12](#)

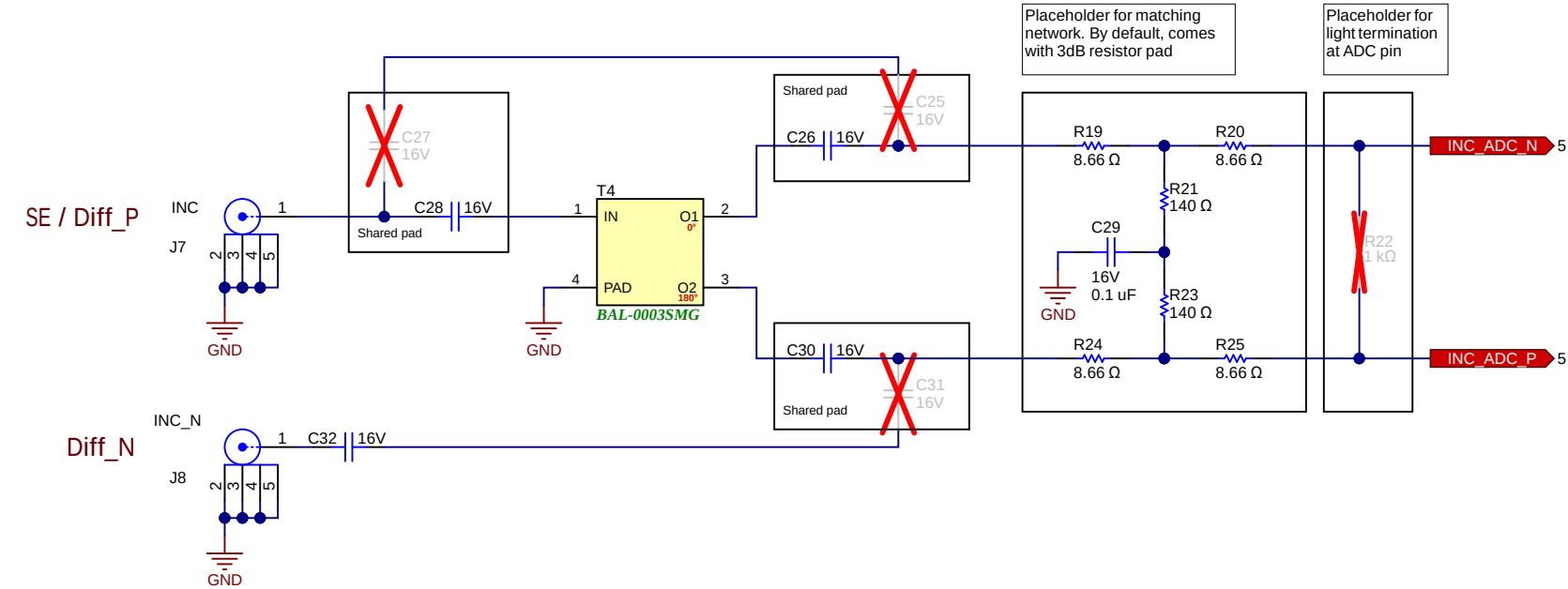


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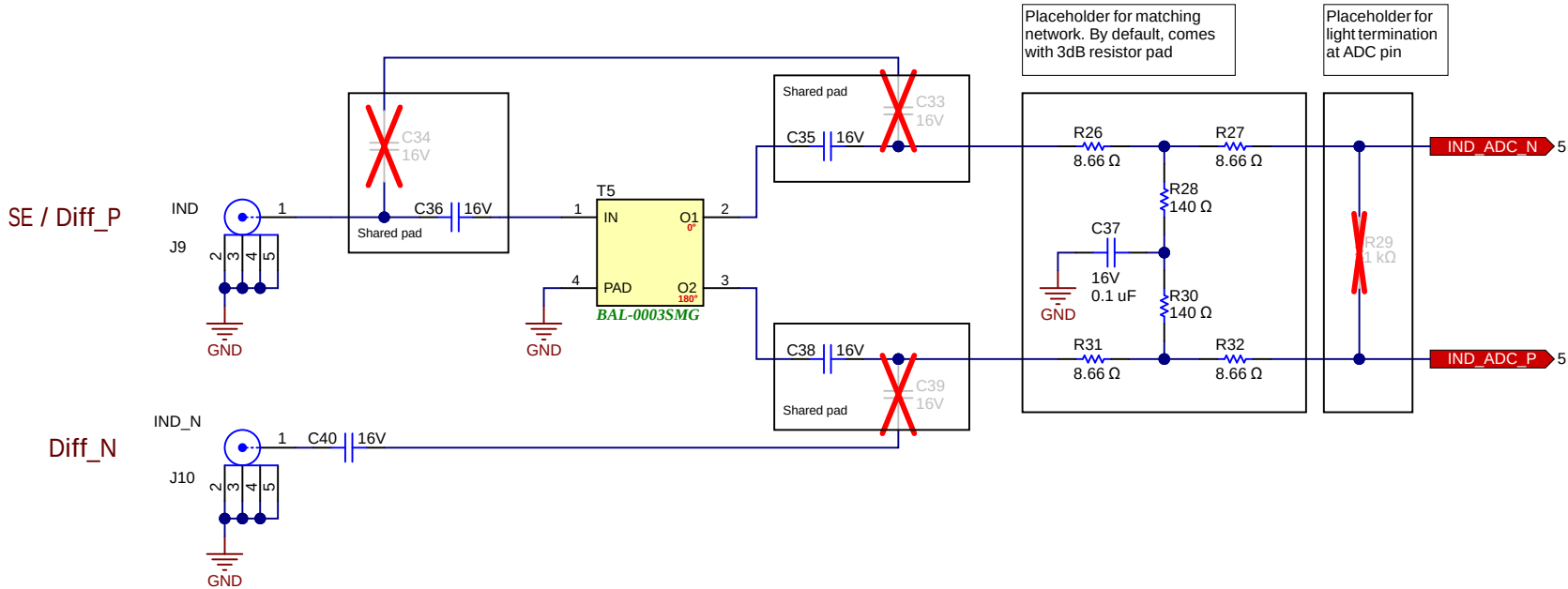
Orderable:	Not For Public Release	Designed for:	Not For Public Release	Mod. Date:	3/3/2025
TID #:	Not For Public Release	Project Title:	ADC34RF7xEVM		
Number:	-	Rev:	A	Sheet Title:	ADC EVM RF Input
SVN Rev:	cfec0883921a2ab84ee9a1a5050b24a5b4522	File:	ADC34RF7x_ADC_Input_AB_RevA.SchDoc	Sheet:	2 of 20
Drawn By:	CW	Size:	B		
Engineer:	CW	Contact:	http://www.ti.com/support		

ADC EVM RF Input

Channel C



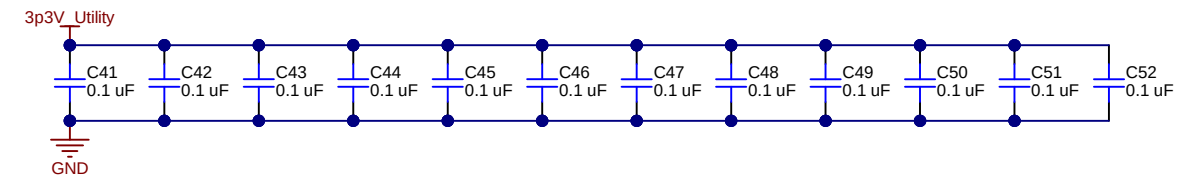
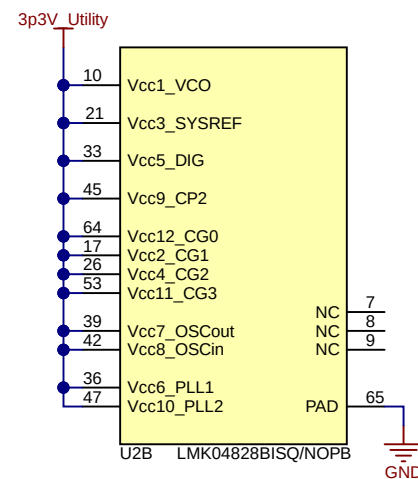
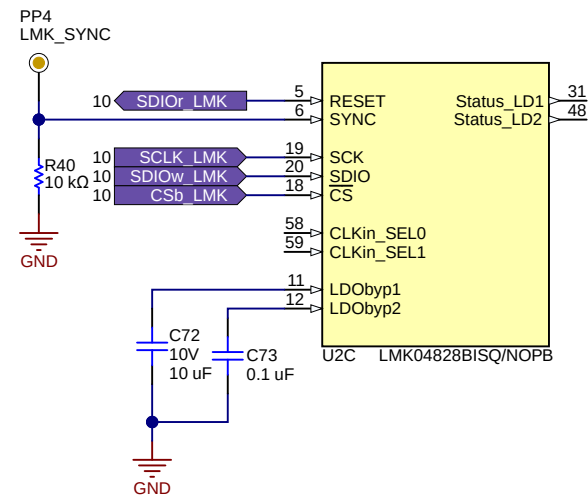
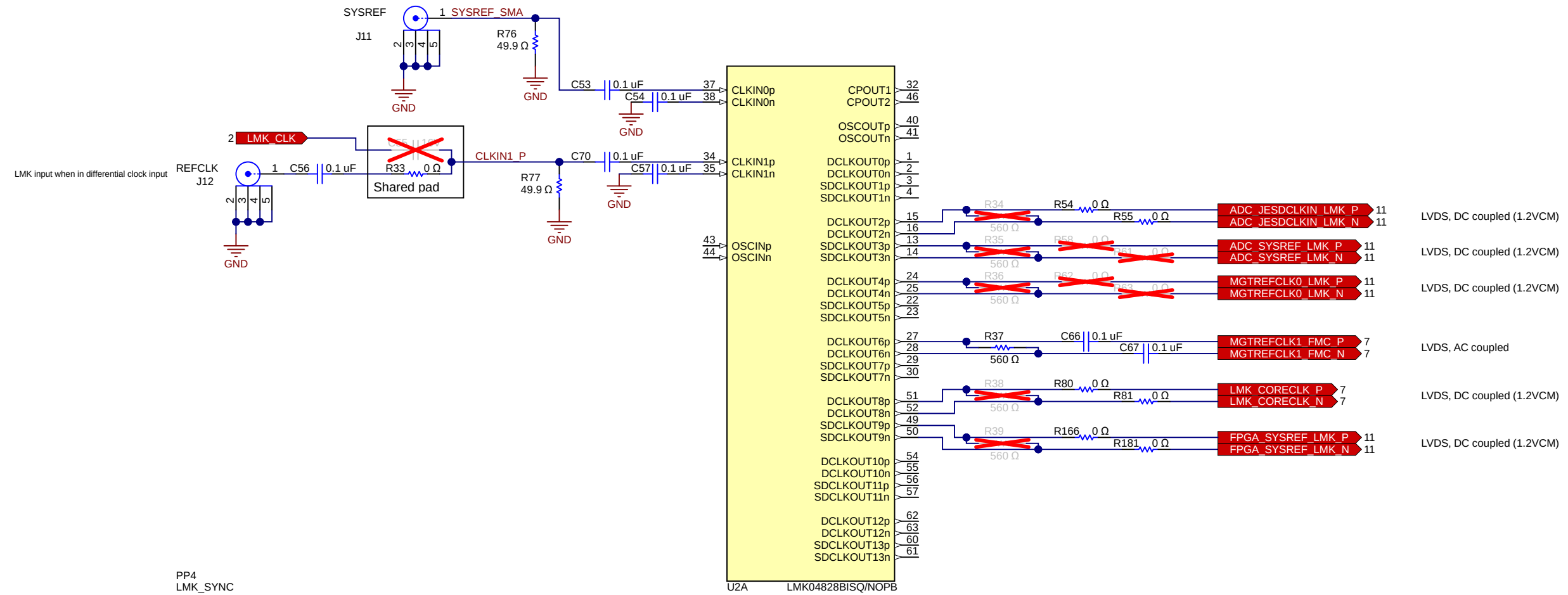
Channel D



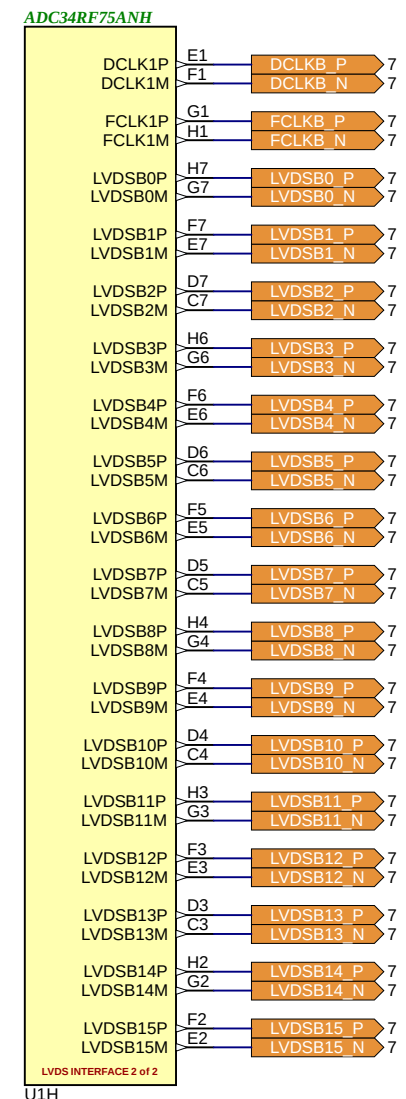
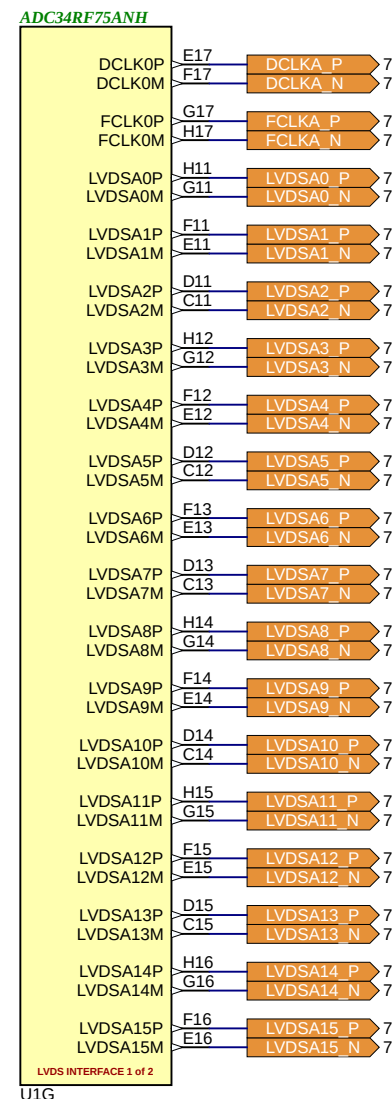
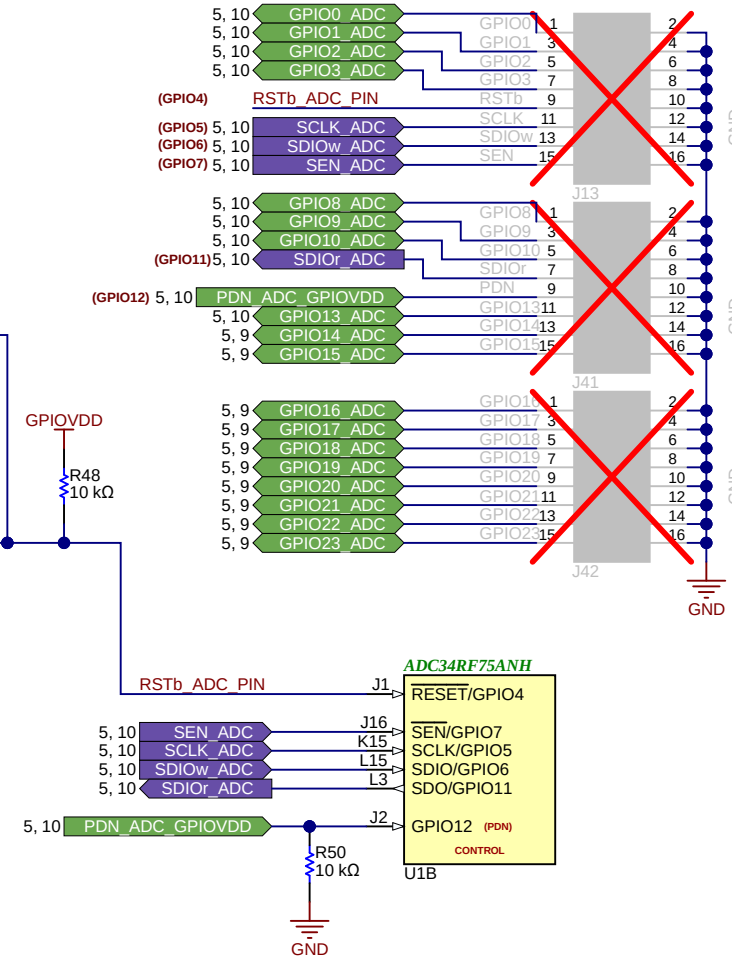
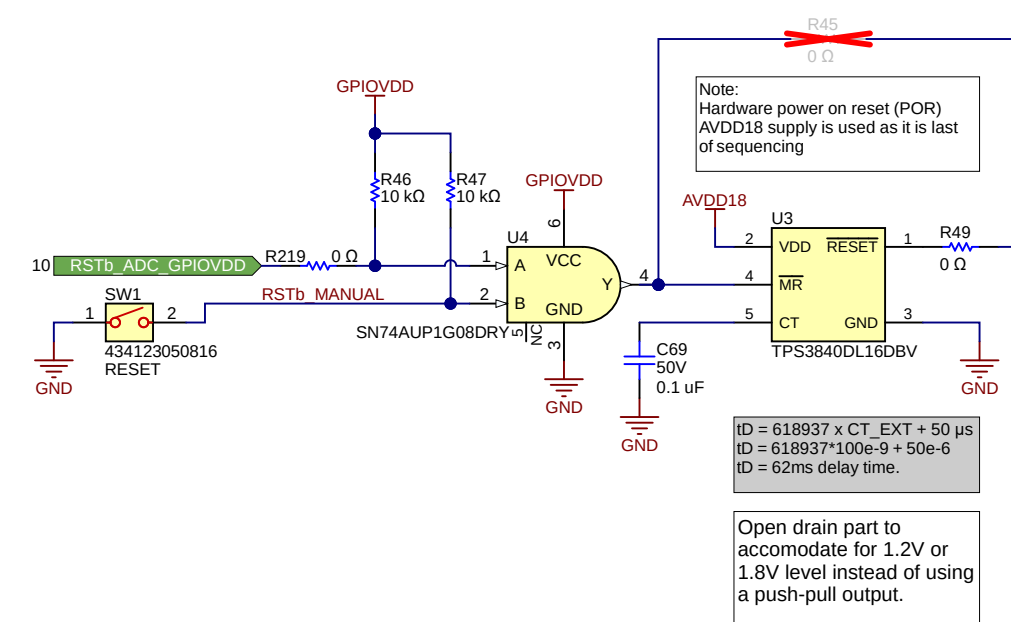
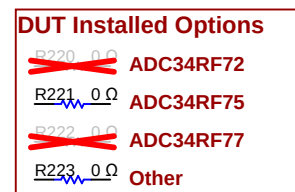
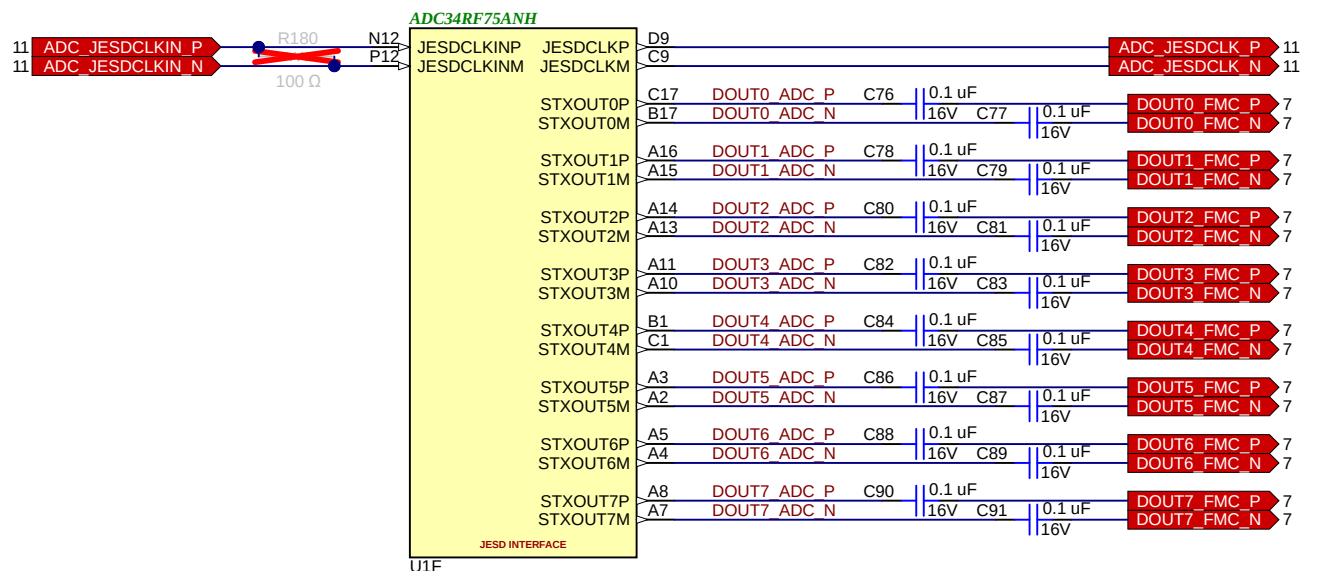
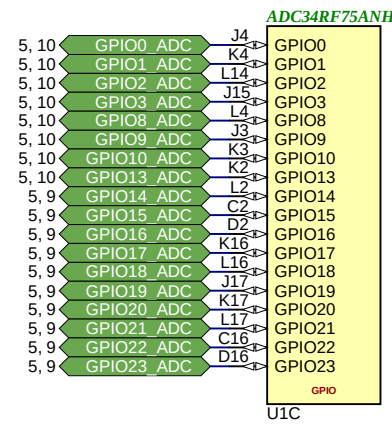
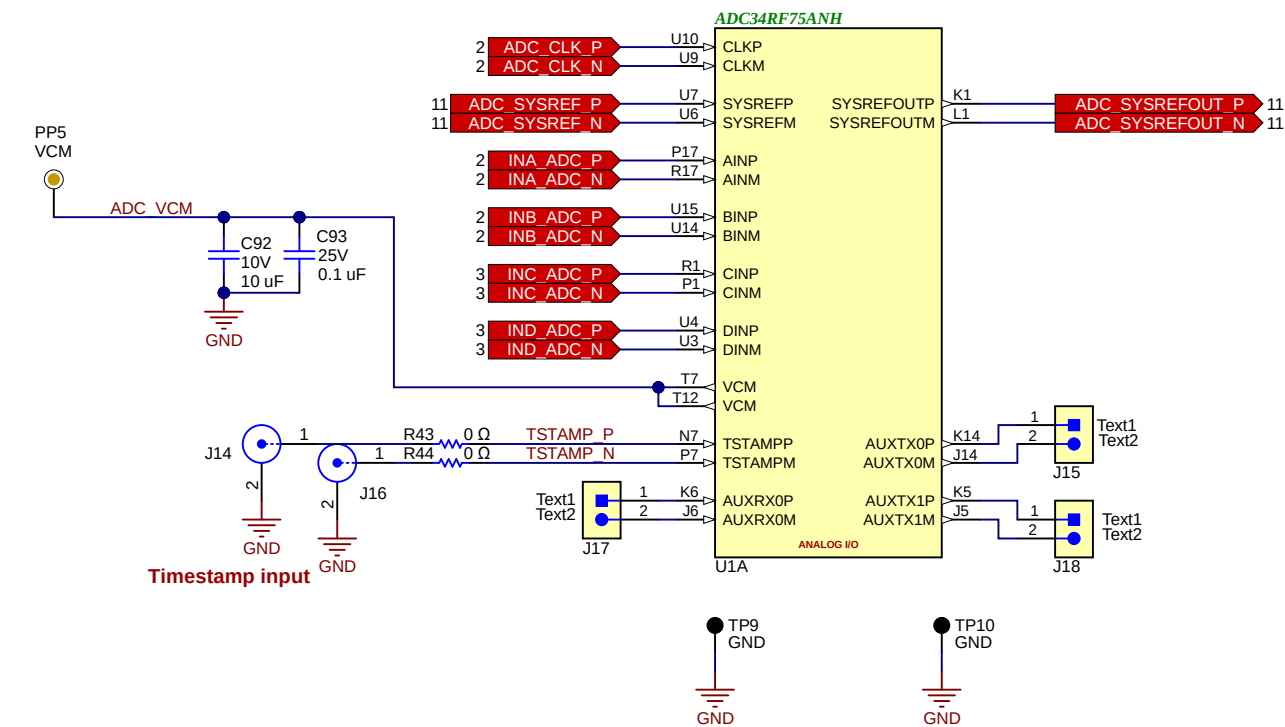
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TID #:	Not For Public Release	Project Title:	ADC34RF7xEVM		
Number:	-	Rev:	A	Sheet Title:	ADC EVM RF Input
SVN Rev:	3549342212367fc0980ad	File:	ADC34RF7x_ADC_Input_CD_RevA.SchDoc	Sheet:	3 of 20
Drawn By:		Engineer:	CW	Size:	B
		Contact:	http://www.ti.com/support		

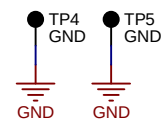
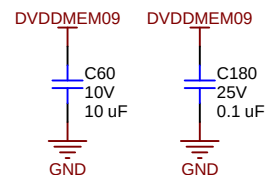
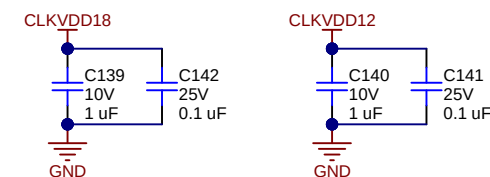
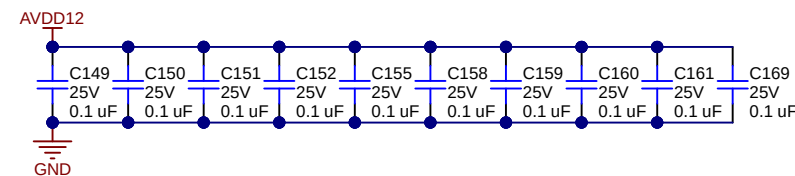
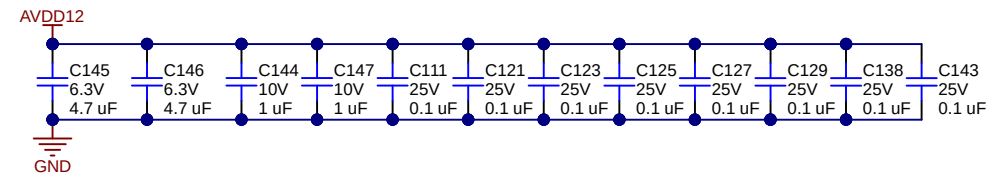
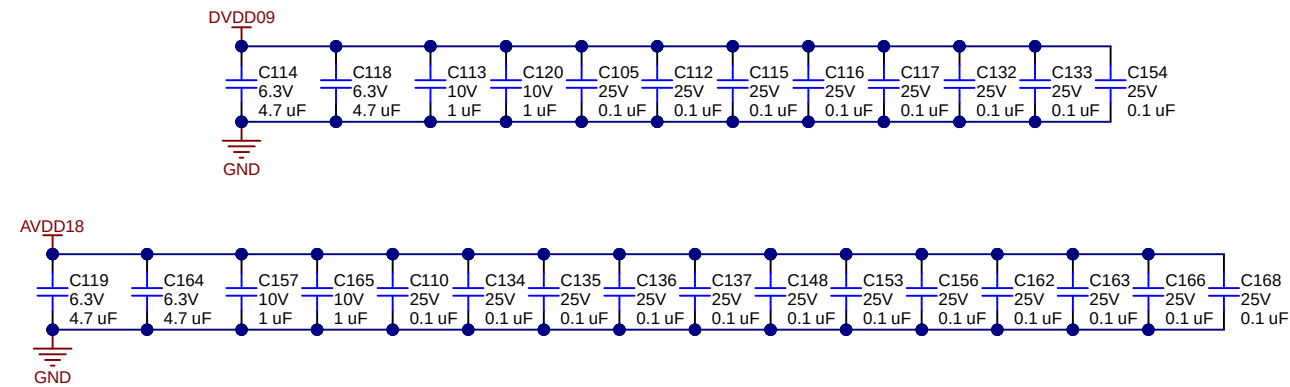
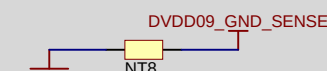
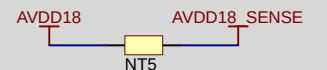
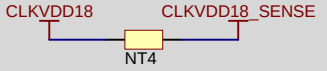
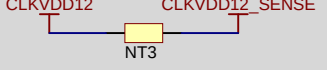
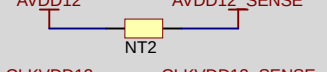
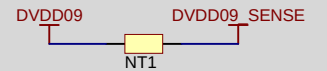
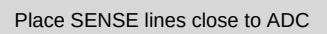
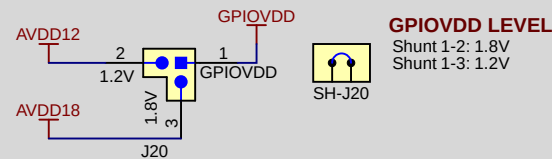
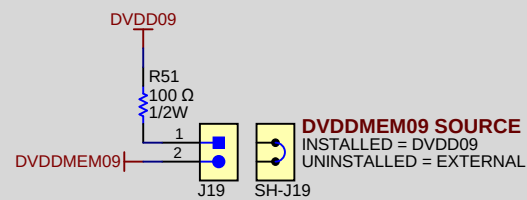
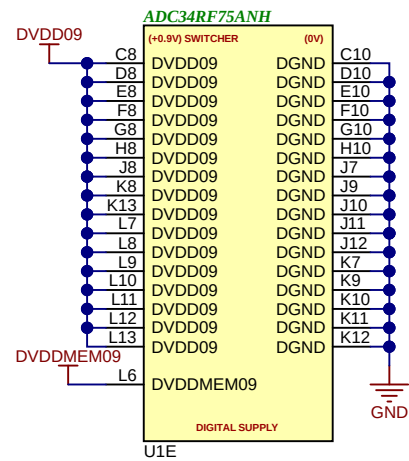
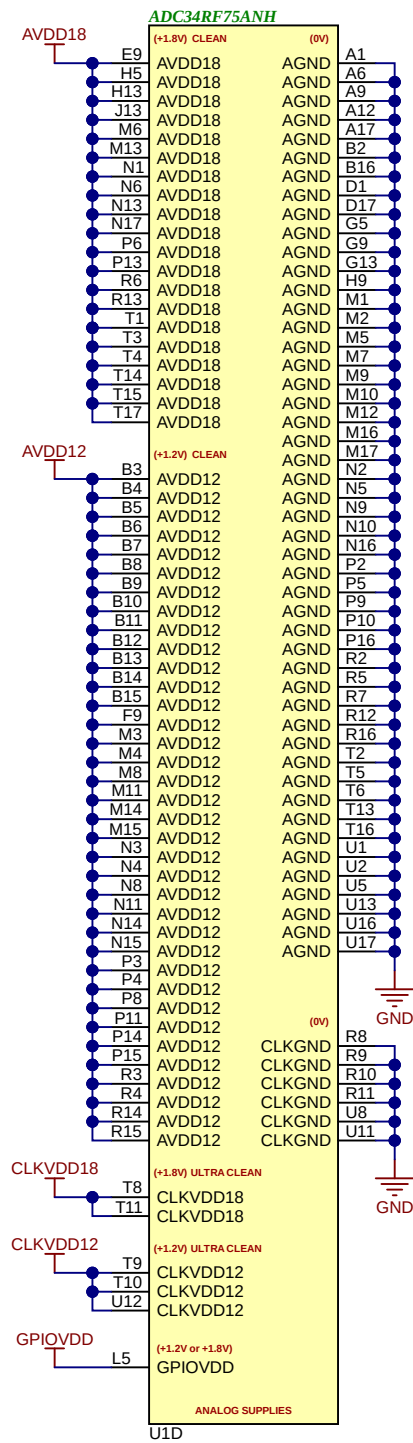
LMK04828 FPGA Clocks and SYSREF



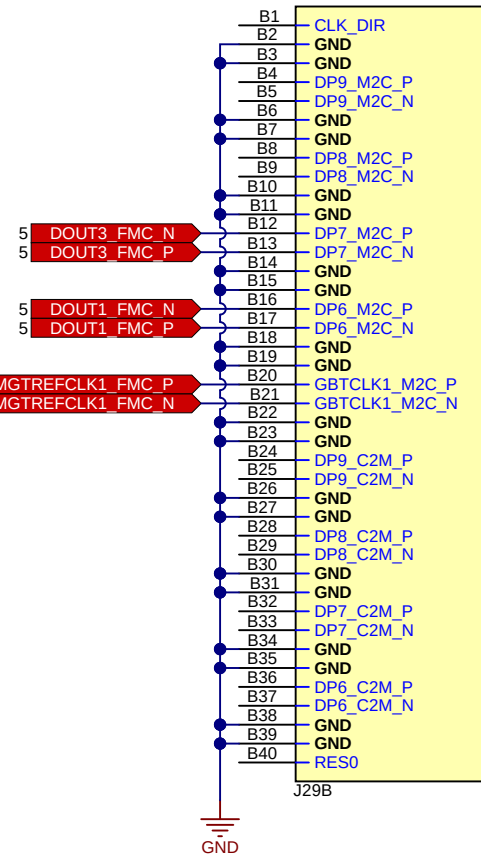
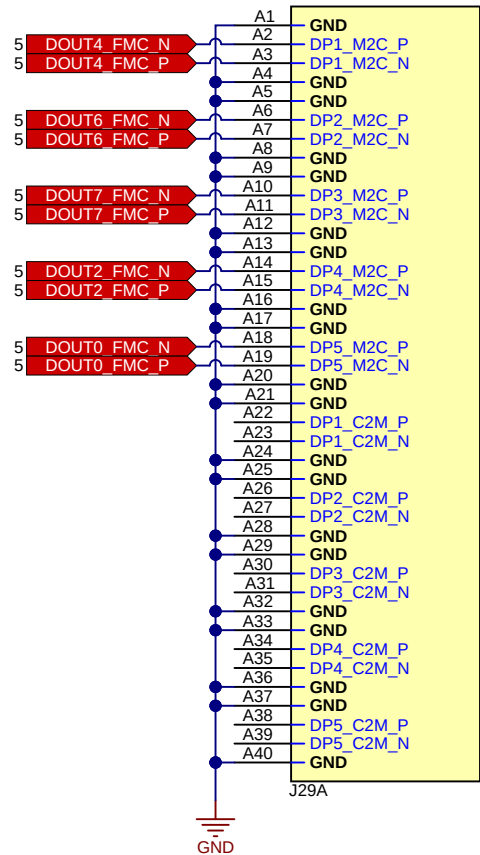
ADC Input, SERDES and Digital Pins



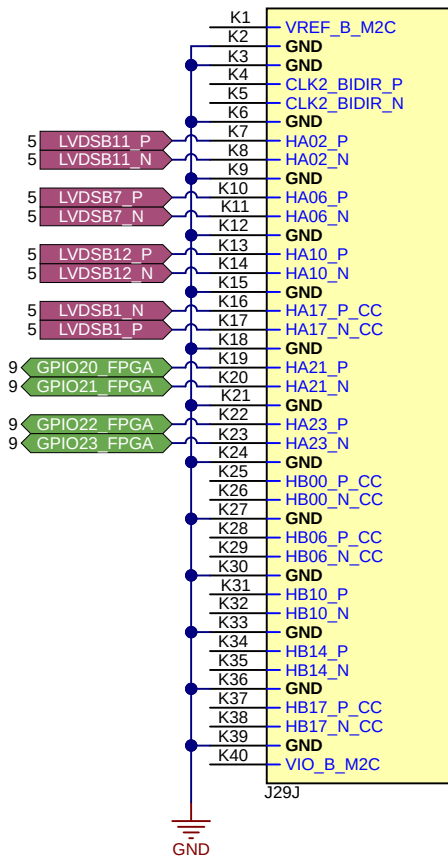
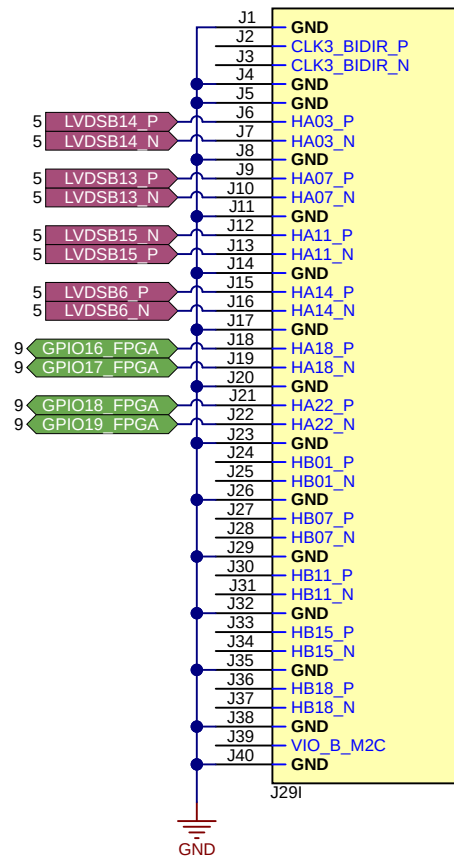
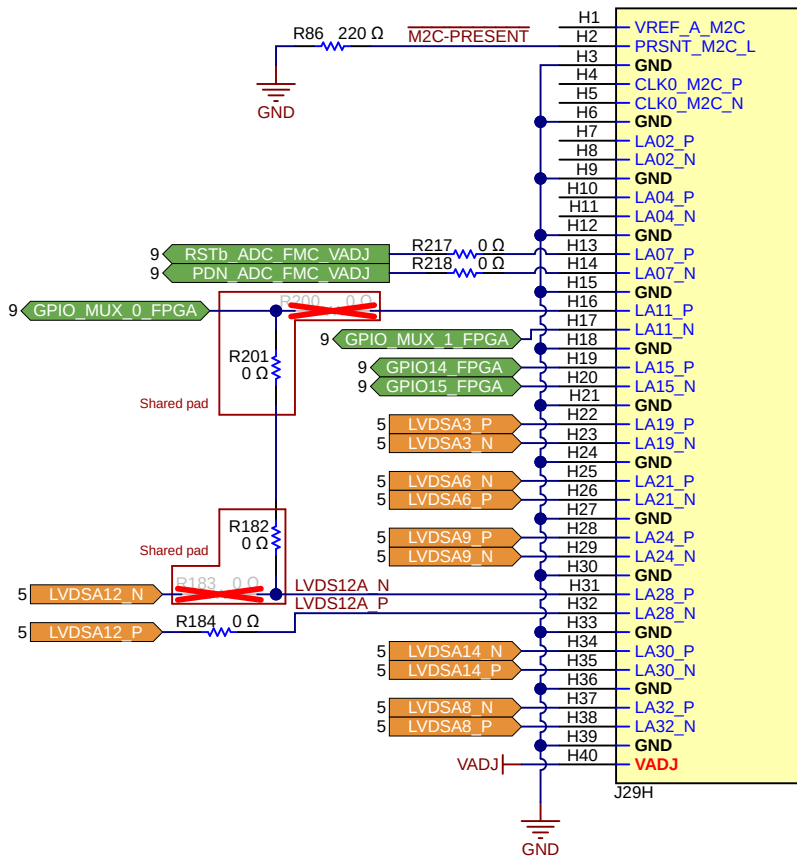
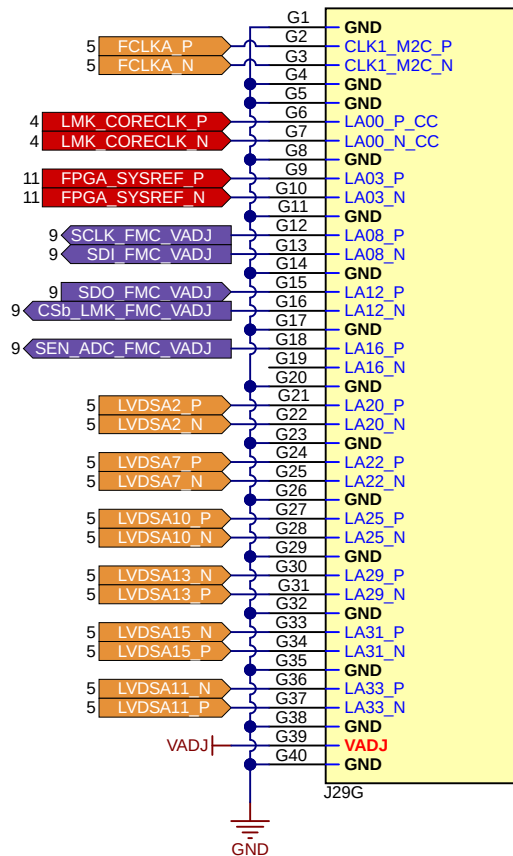
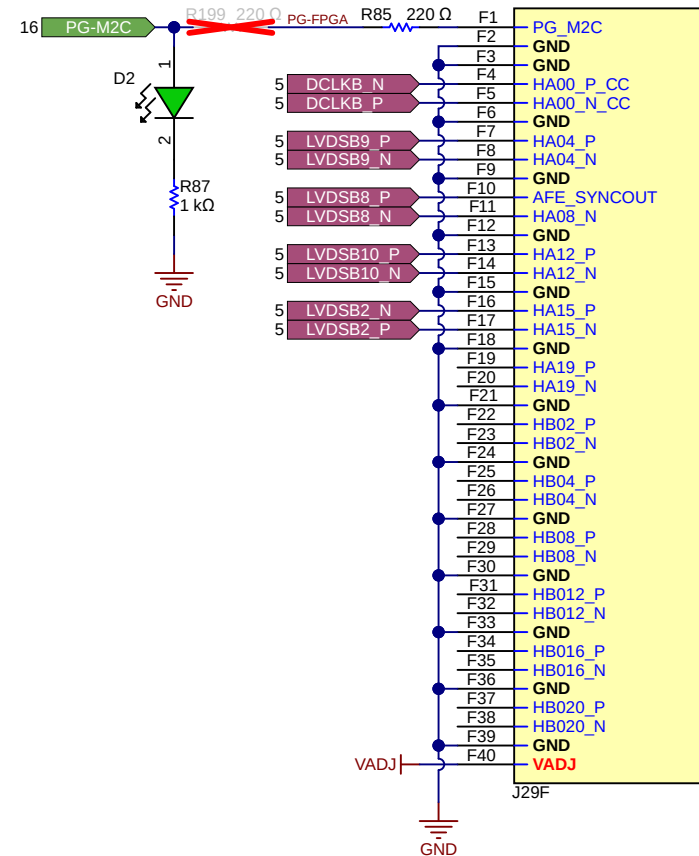
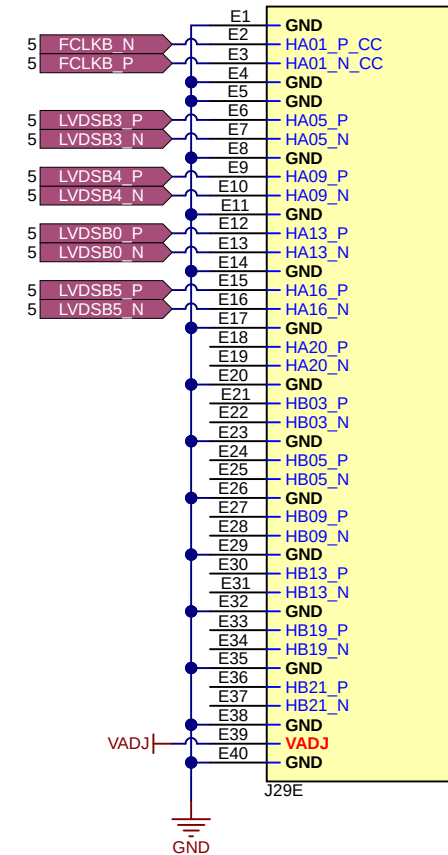
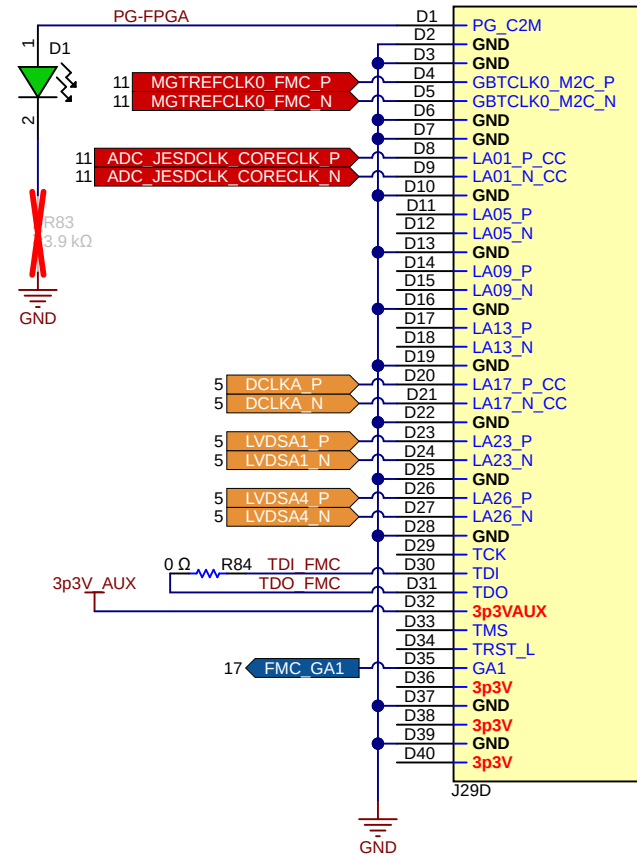
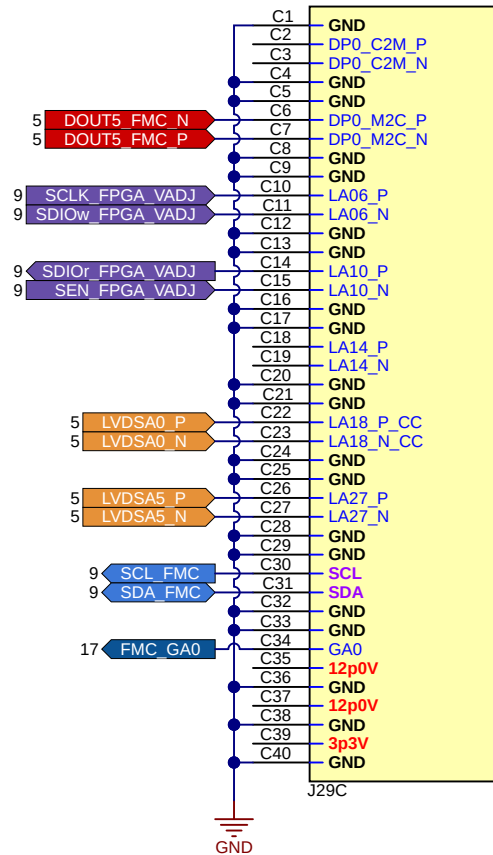
ADC EVM Power



FMC Connector



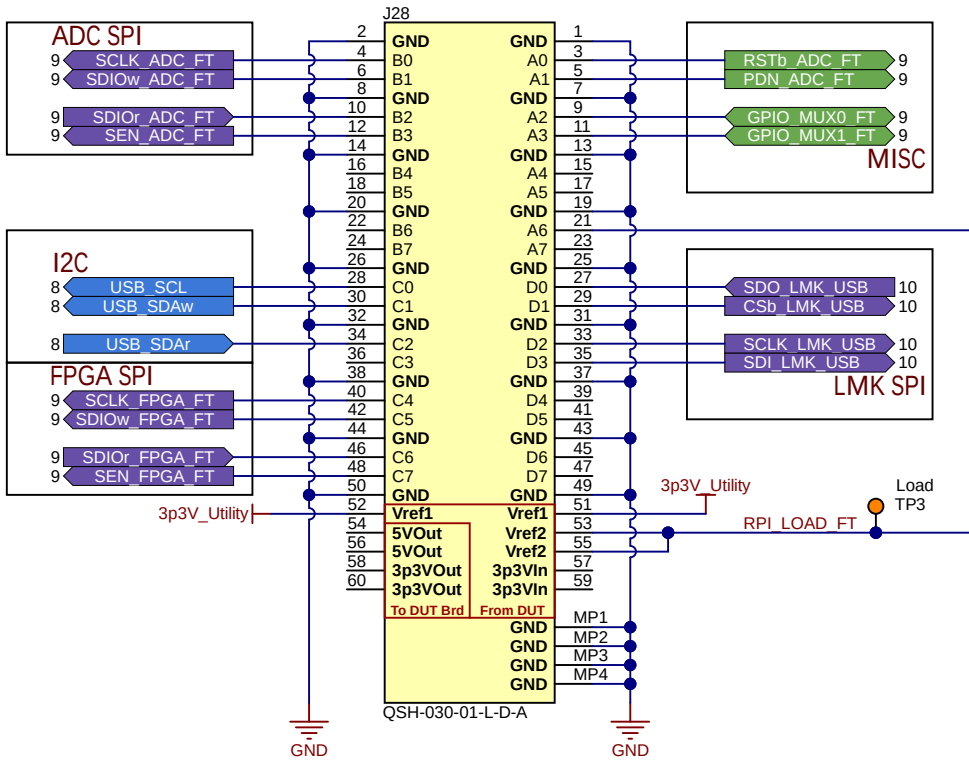
FPGA as SPI Peripheral



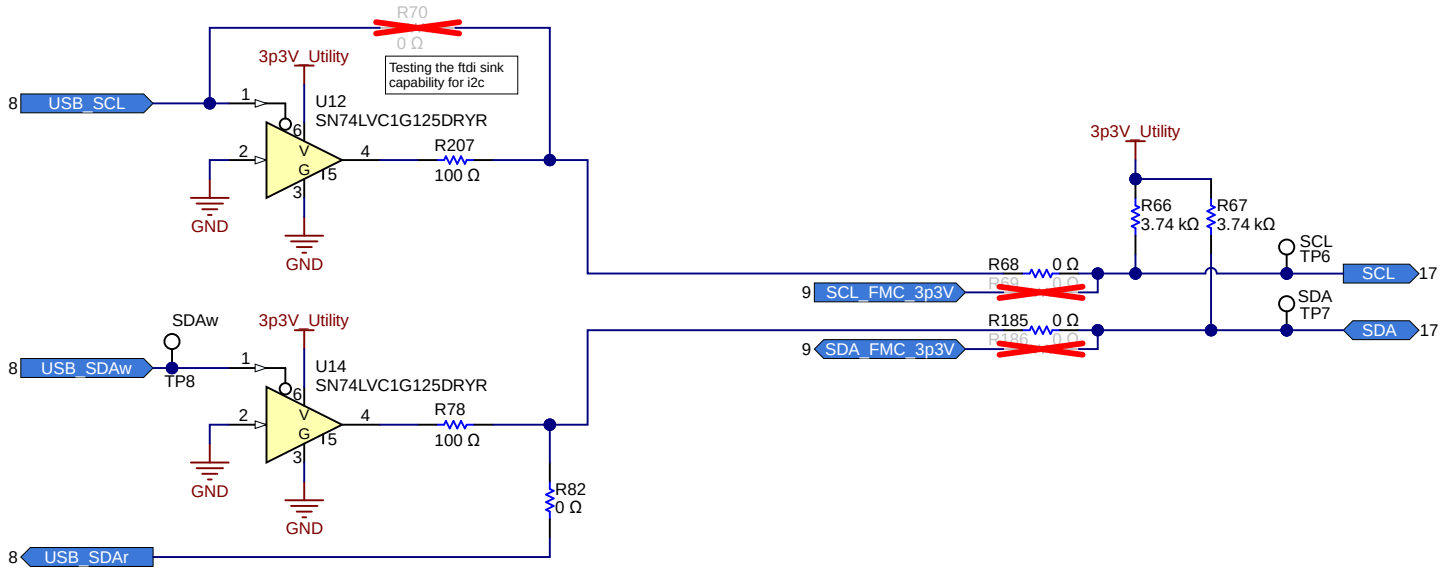
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Note: FTDI pinout matches TII dualsite board for ADC(site1) & LMK

*Note: All SDIO naming convention is from the perspective of the FTDI host controller.
SDIOw = Serial Data In (FTDI → ADC/LMK)
SDIOr = Serial Data Out (ADC/LMK → FTDI)

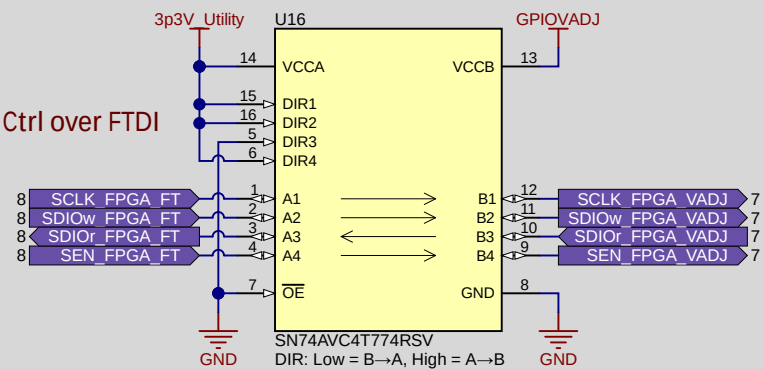


Vref1: Passes 3.3V to RPi autload board



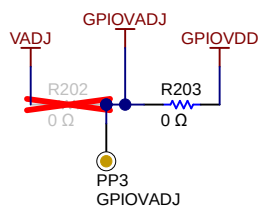
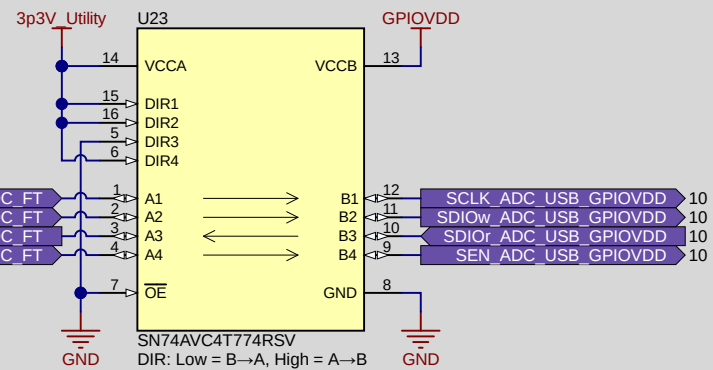
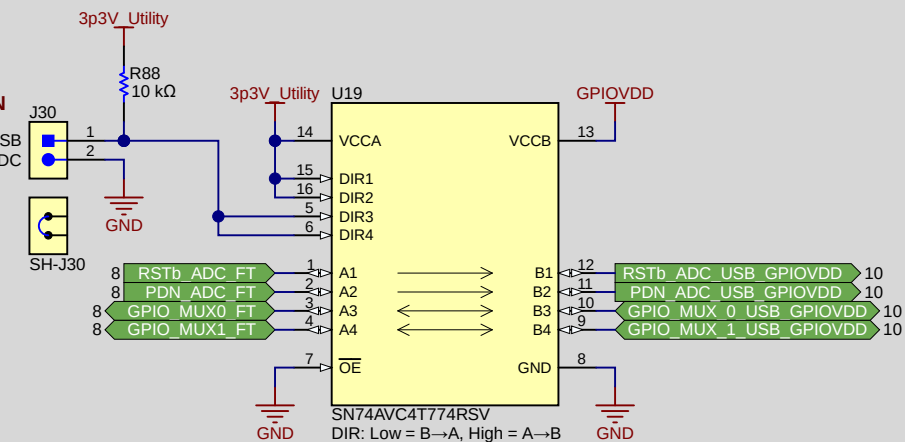
FTDI Level Shifting

FPGA Ctrl over FTDI

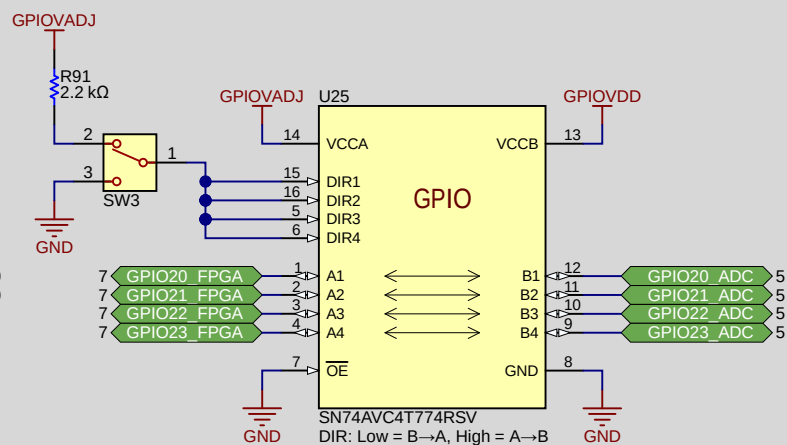
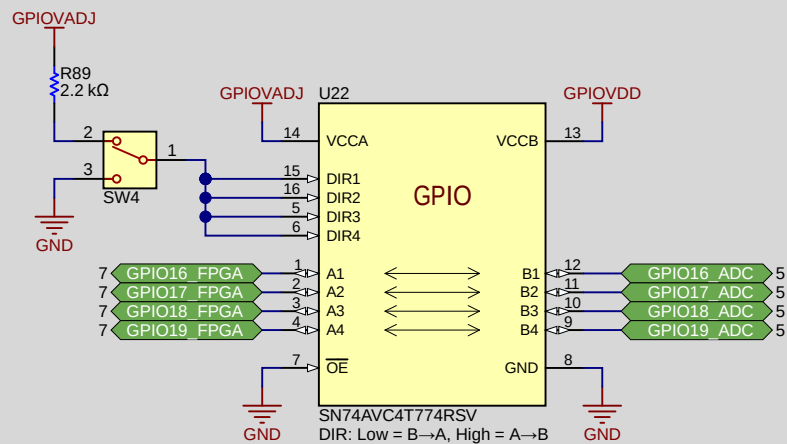
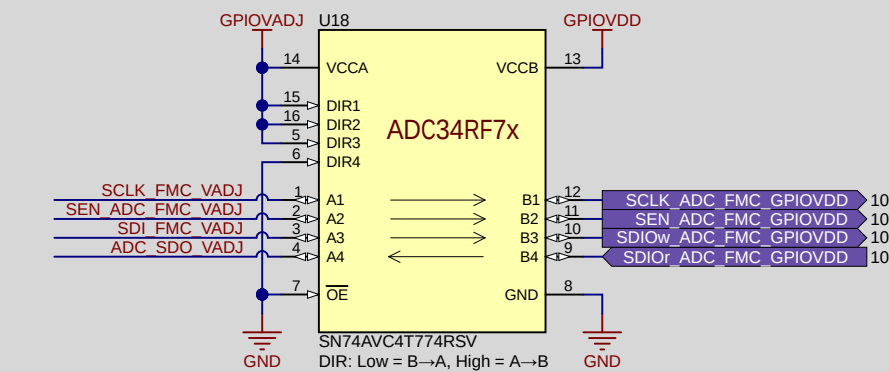
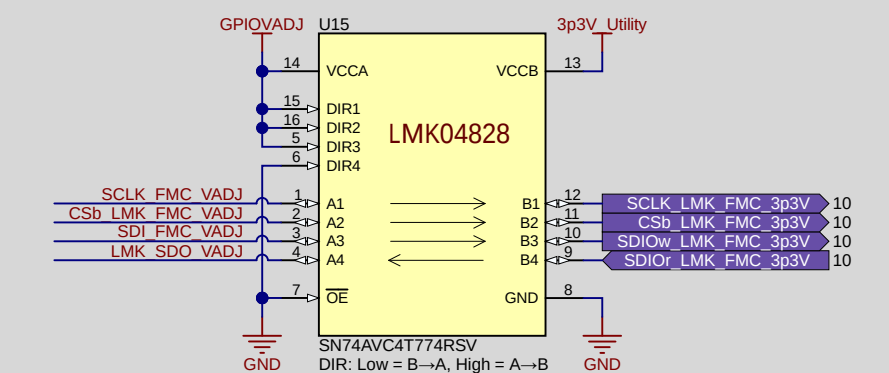
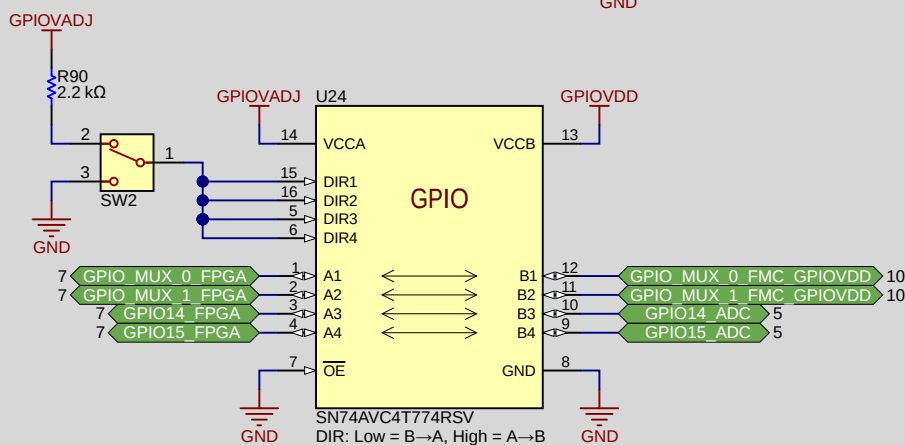
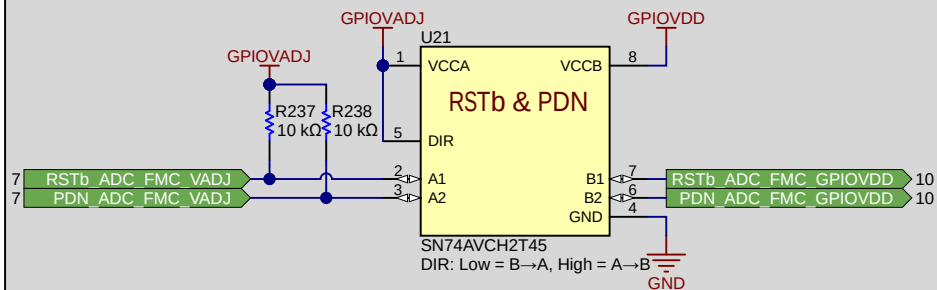
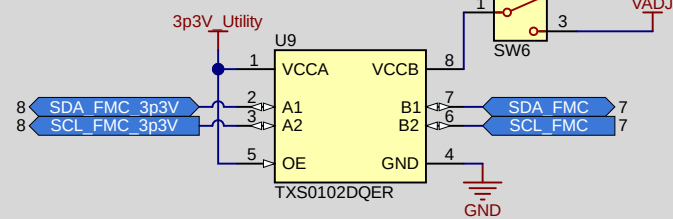
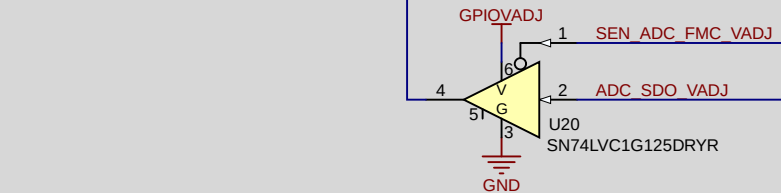
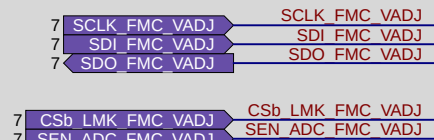


USB GPIO DIRECTION

INSTALLED = ADC to USB
UNINSTALLED = USB to ADC



FPGA Level Shifting



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Orderable: Not For Public Release	Designed for: Not For Public Release	Mod. Date: 3/13/2025
TID #: Not For Public Release	Project Title: ADC34RF7xEVM	
Number: -	Rev: A	Sheet Title: Level Shifting
SVN Rev: cfc0883921a2ab84ee9a1a505022-ADC34RF75	Sheet: 9 of 20	
Drawn By: CW	File: ADC34RF7x_LVL_Shift_RevA.SchDoc	Size: B
Engineer: CW	Contact: http://www.ti.com/support	

MUXes

A

B

C

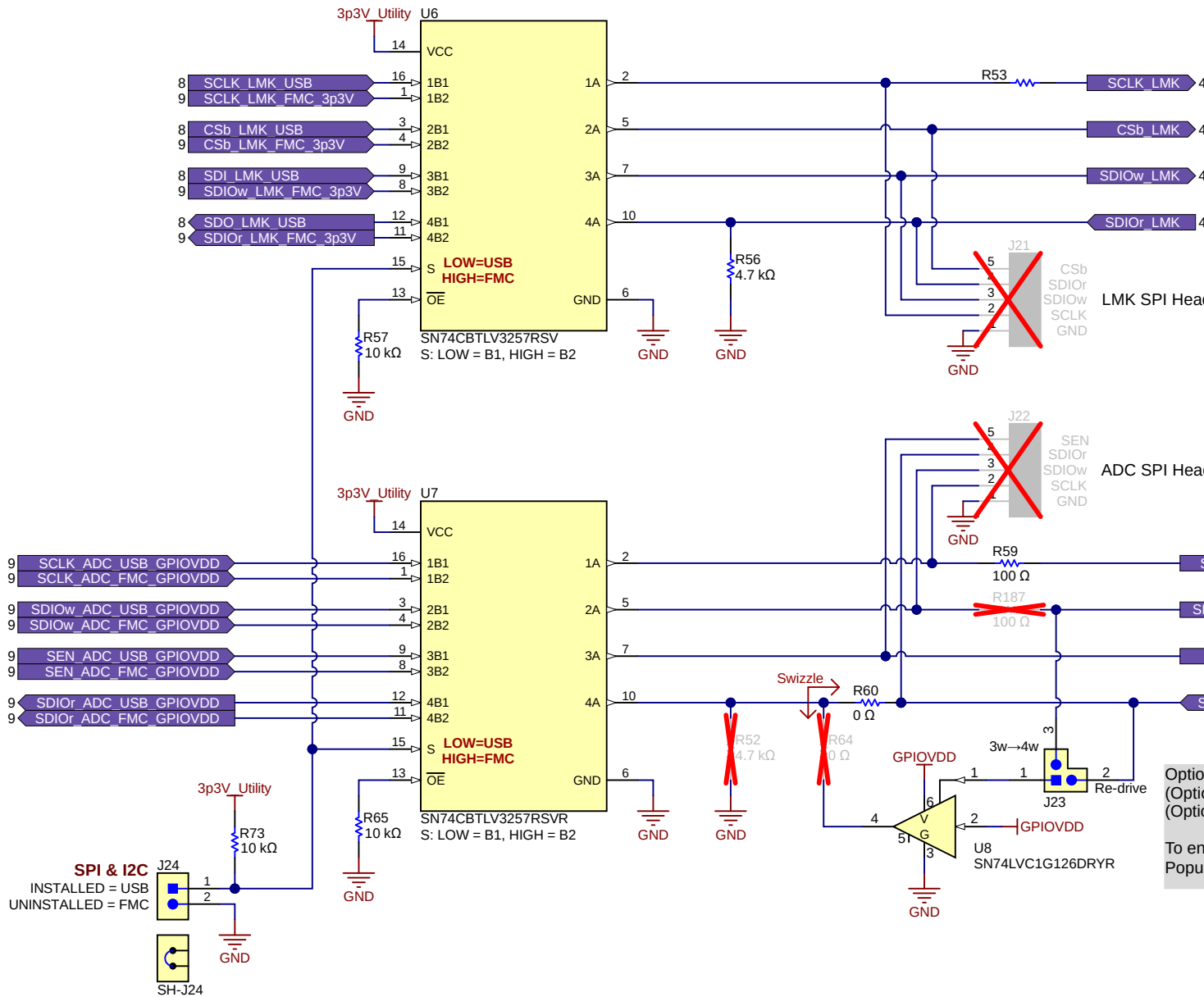
D

A

B

C

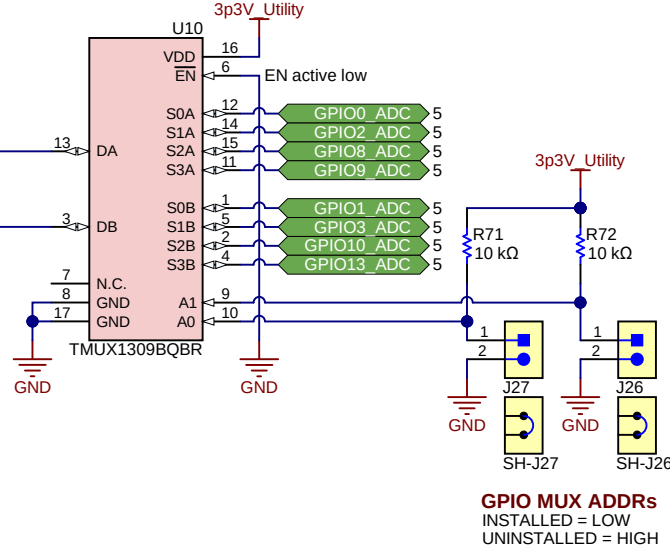
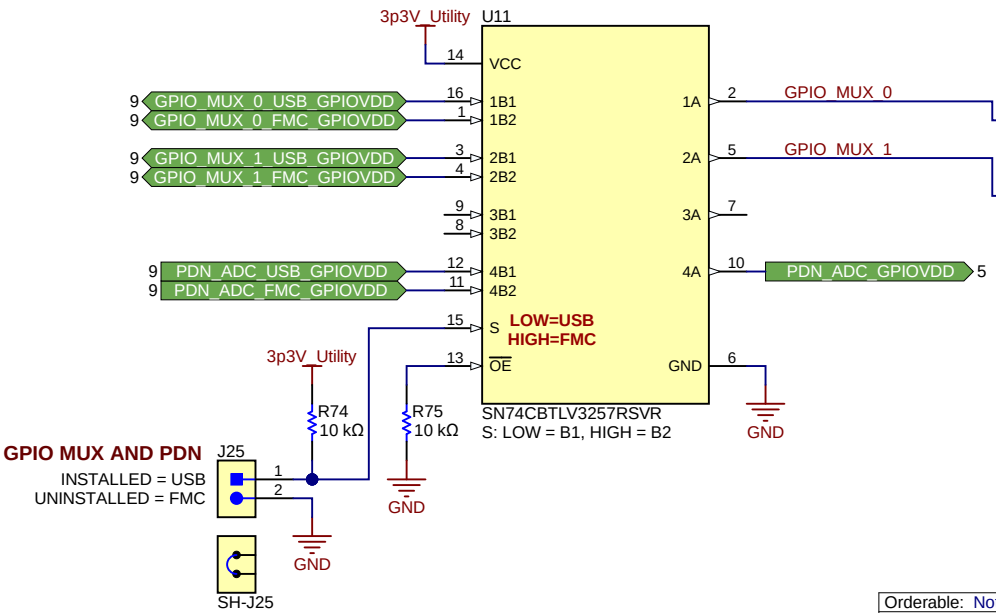
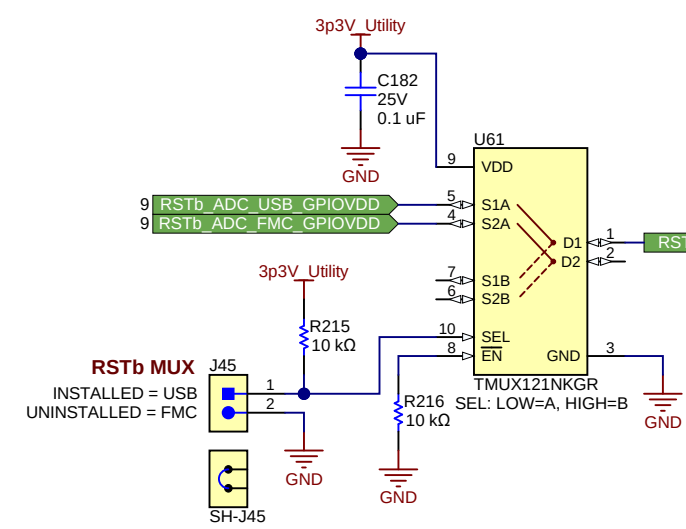
D



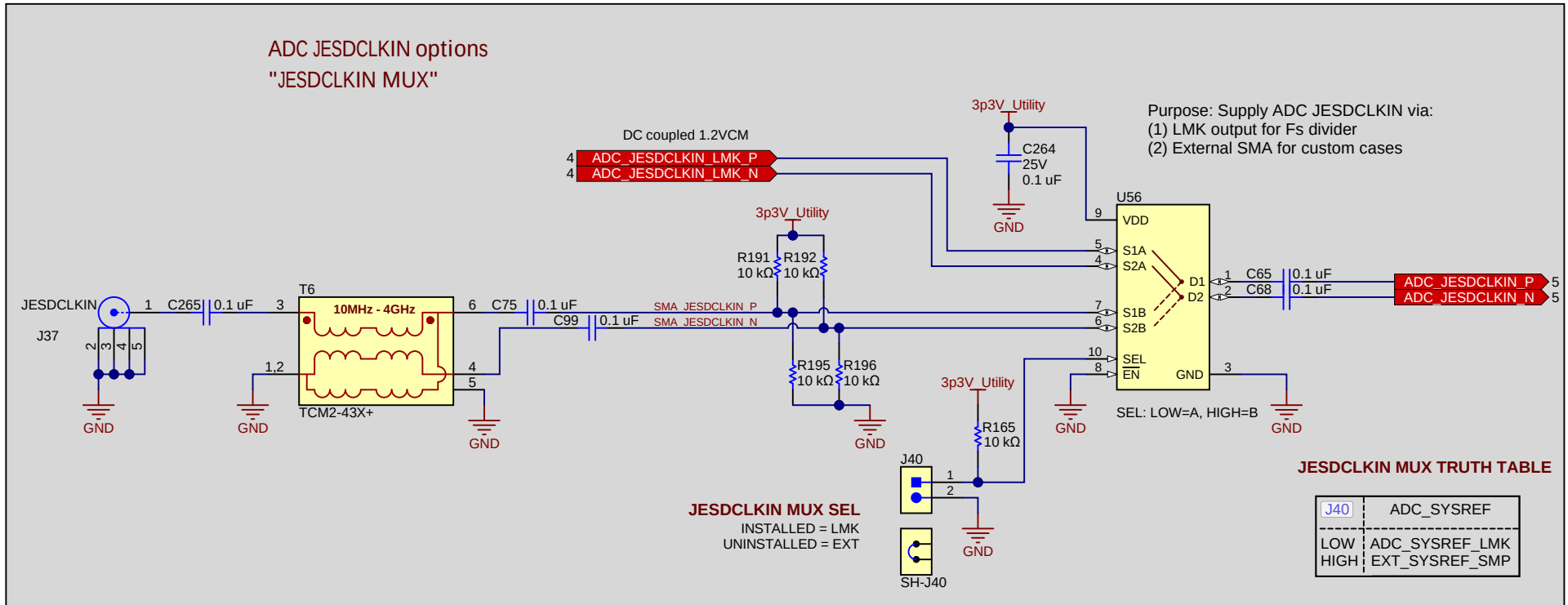
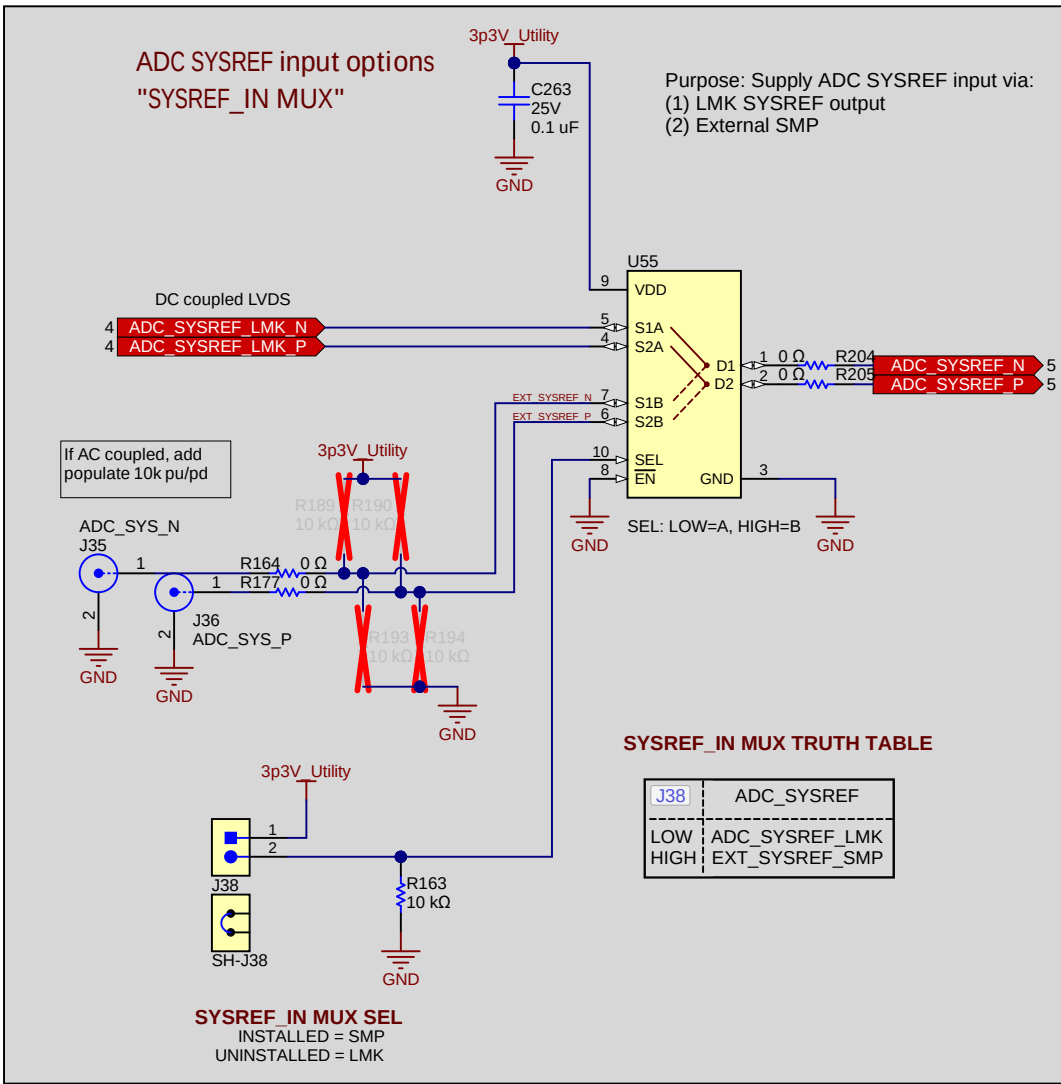
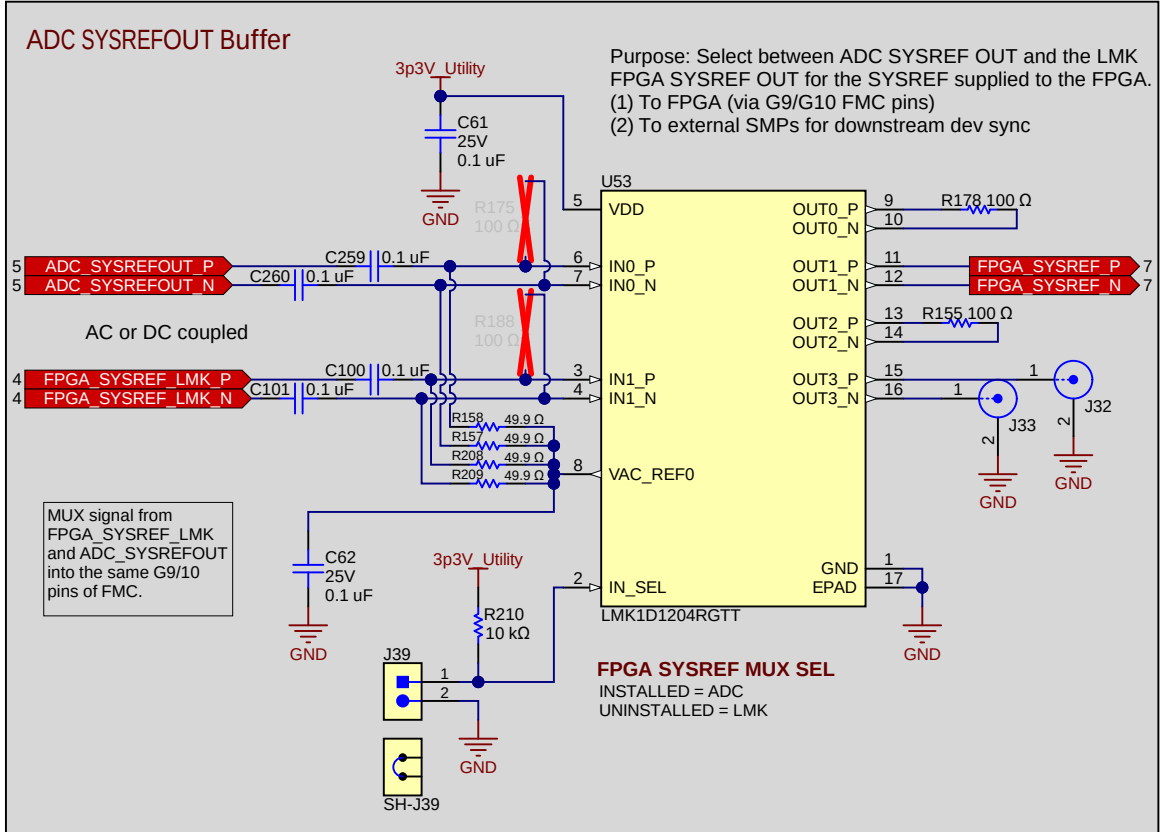
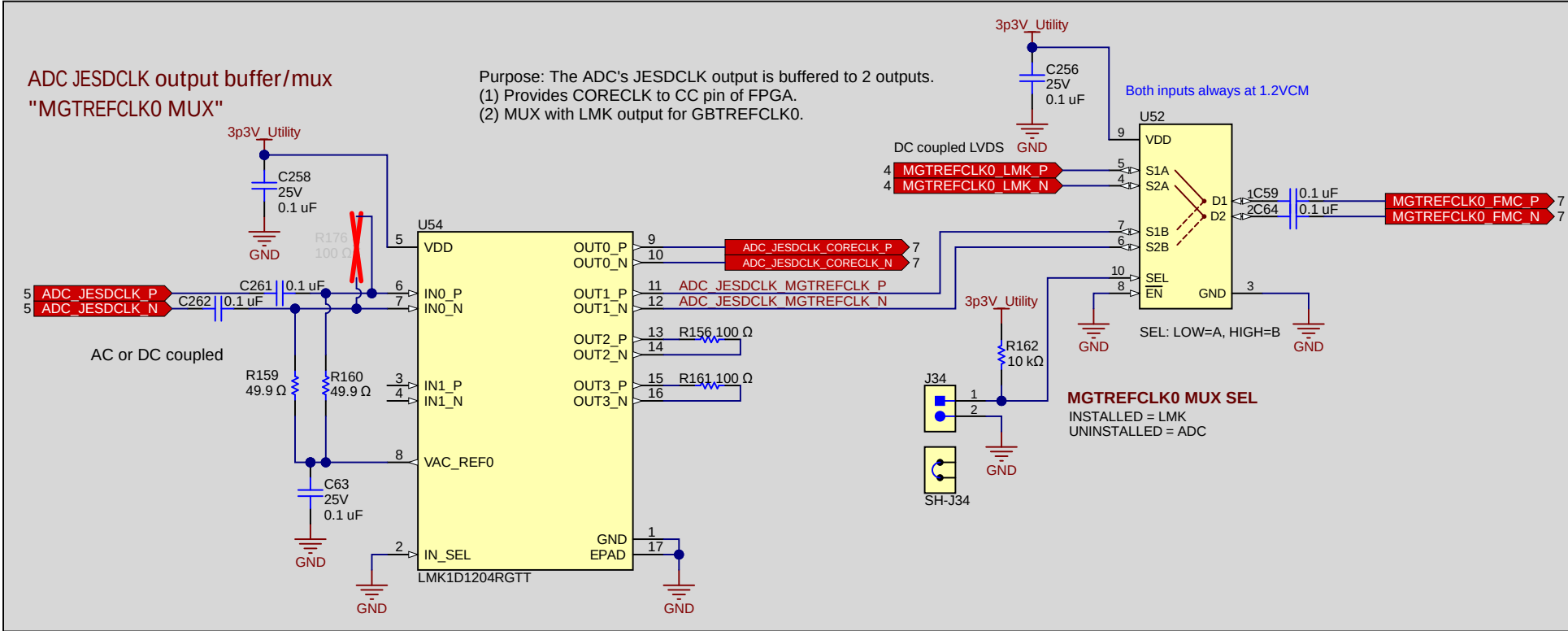
Optional buffer serves 2 purposes:
(Optional) 3w → 4w SPI conversion (1-3)
(Optional) ADC SDO re-driver (1-2)

To enable buffer usage for either case:
Populate **R64** and depopulate **R60**

GPIO MUX TRUTH TABLE			
J27	J26	GPIO_MUX_0	GPIO_MUX_1
LOW	LOW	GPIO0_ADC	GPIO8_ADC
LOW	HIGH	GPIO1_ADC	GPIO9_ADC
HIGH	LOW	GPIO2_ADC	GPIO10_ADC
HIGH	HIGH	GPIO3_ADC	GPIO13_ADC

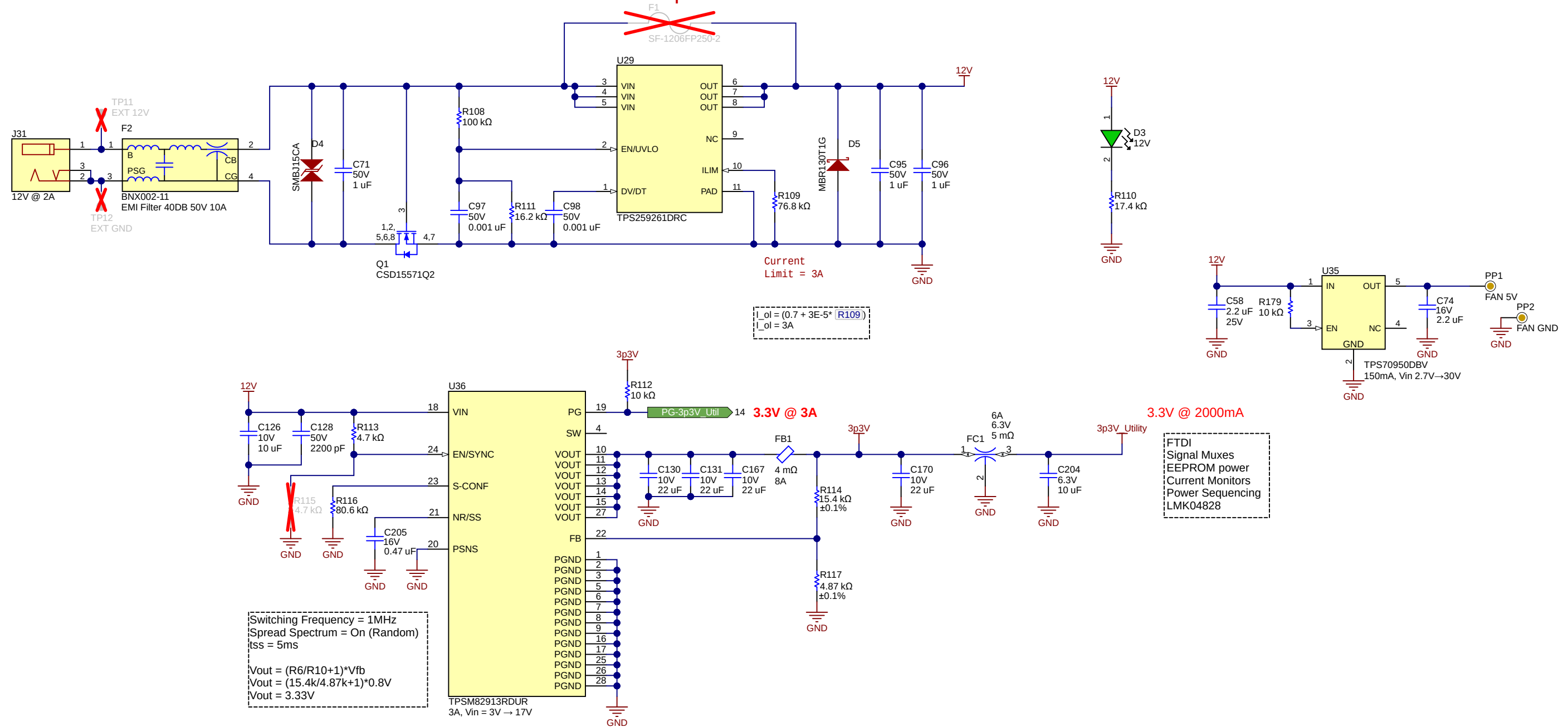


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POWER UP SEQUENCE

1. DVDD (0.9V)
2. AVDD12 (1.2V) → CLKVDD12 (1.2V)
3. AVDD18 (1.8V) → CLKVDD18 (1.8V)

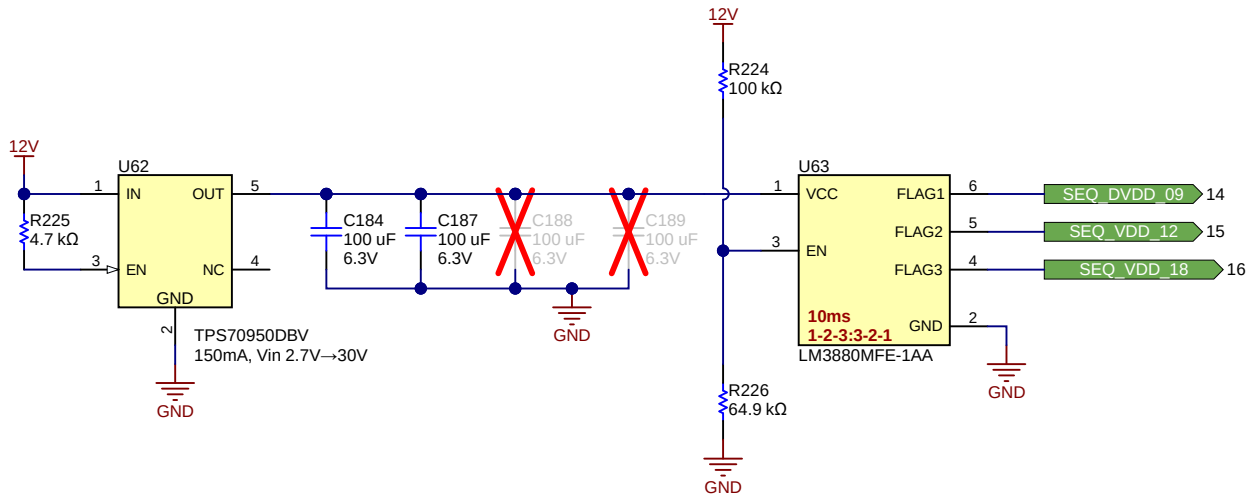


Switching Frequency = 1MHz
Spread Spectrum = On (Random)
tss = 5ms

$V_{out} = (R6/R10+1)*V_{fb}$
 $V_{out} = (15.4k/4.87k+1)*0.8V$
 $V_{out} = 3.33V$

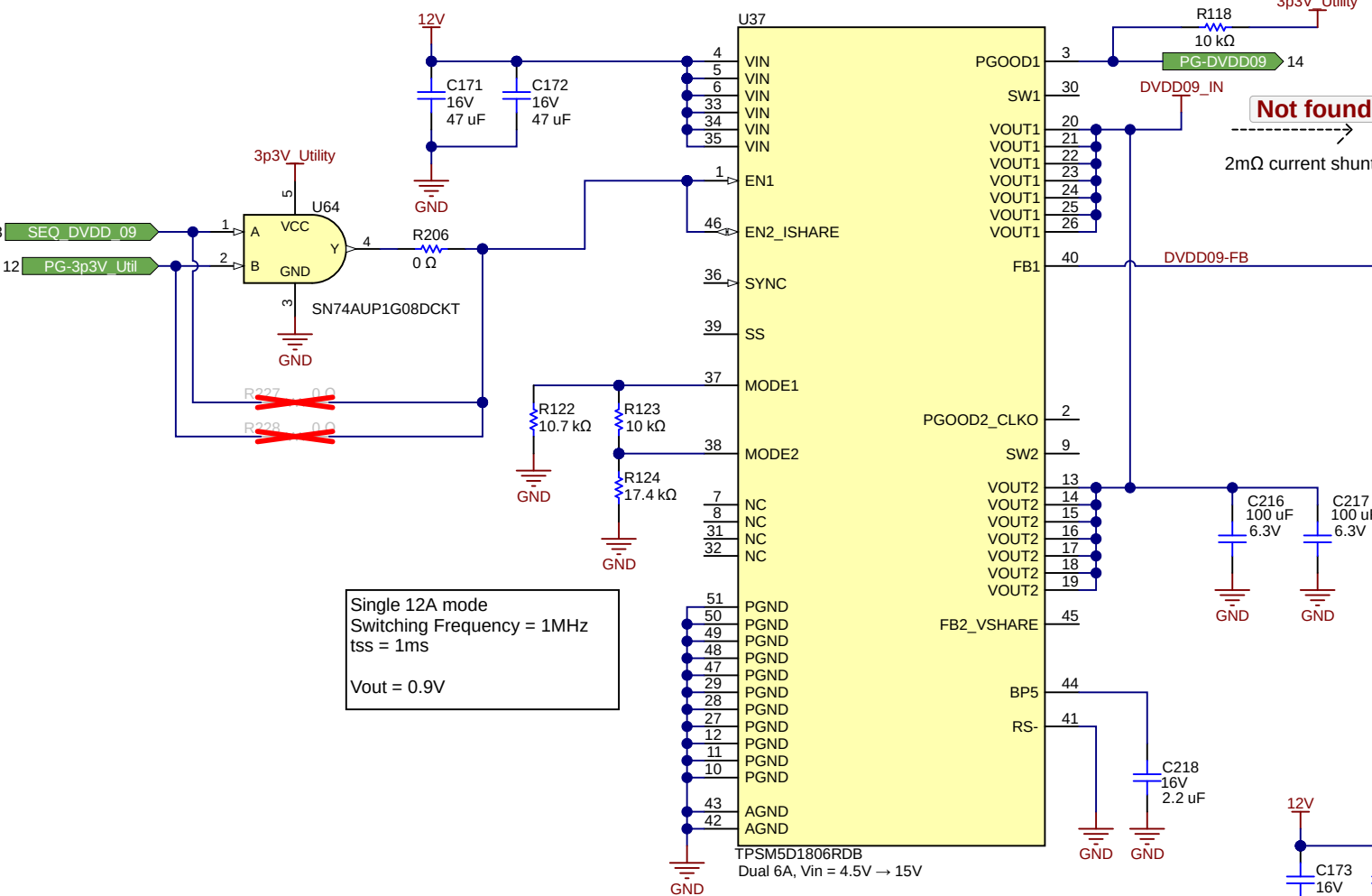
FTDI
Signal Muxes
EEPROM power
Current Monitors
Power Sequencing
LMK04828

Power Sequencer



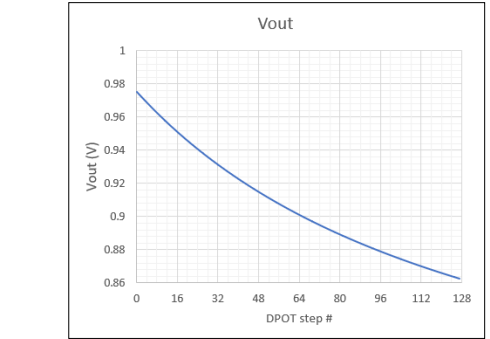
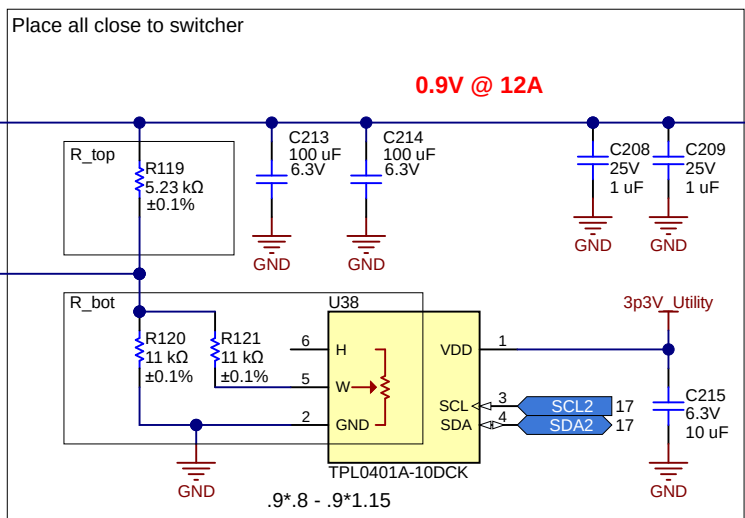
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EVM Power 2
DVDD09, DC-DC before LDOs



Single 12A mode
Switching Frequency = 1MHz
tss = 1ms
Vout = 0.9V

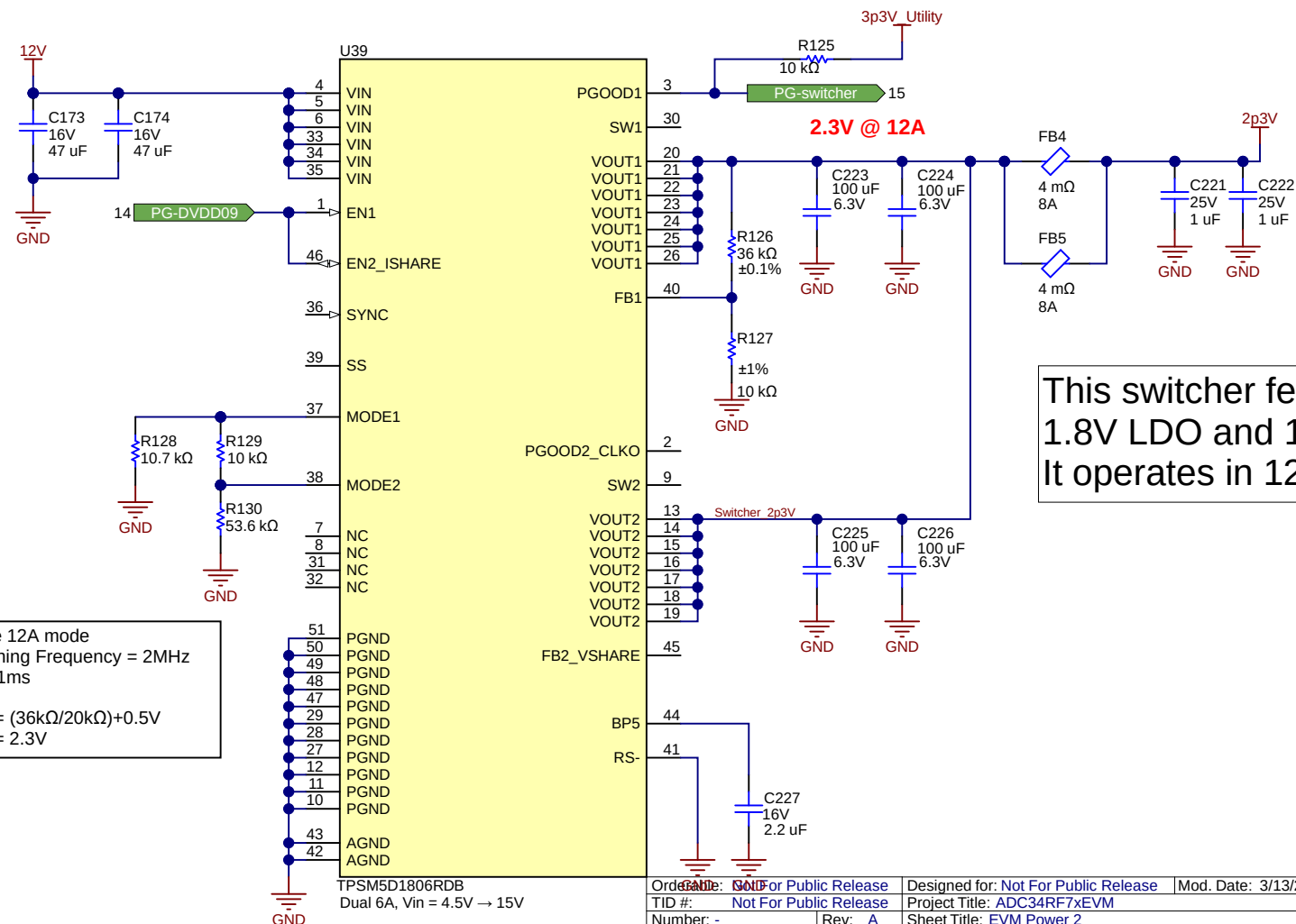
To switch over to uFit power connector, break **R206**, **R119** and **Not found** (2mΩ current shunt) for DVDD



$R_{bot} = 11k\Omega // (11k\Omega + 5k\Omega) = 6.518k\Omega$
 $V_{out} = (5.23k\Omega / (2 * 6.518k\Omega) + 0.5) * 0.901V$
 $R_{wiper} = 10k\Omega; R_{bot} = 7.218k\Omega, V_{out} = 0.862V$
 $R_{wiper} = 0\Omega; R_{bot} = 5.5k\Omega, V_{out} = 0.975V$
Resolution at mid-scale $\approx 8\mu V$

R_wiper refers to R_WL (Resistance from pin 5 to pin 2)

**TODO change feedback res values to achieve 0.7V through 1.1V

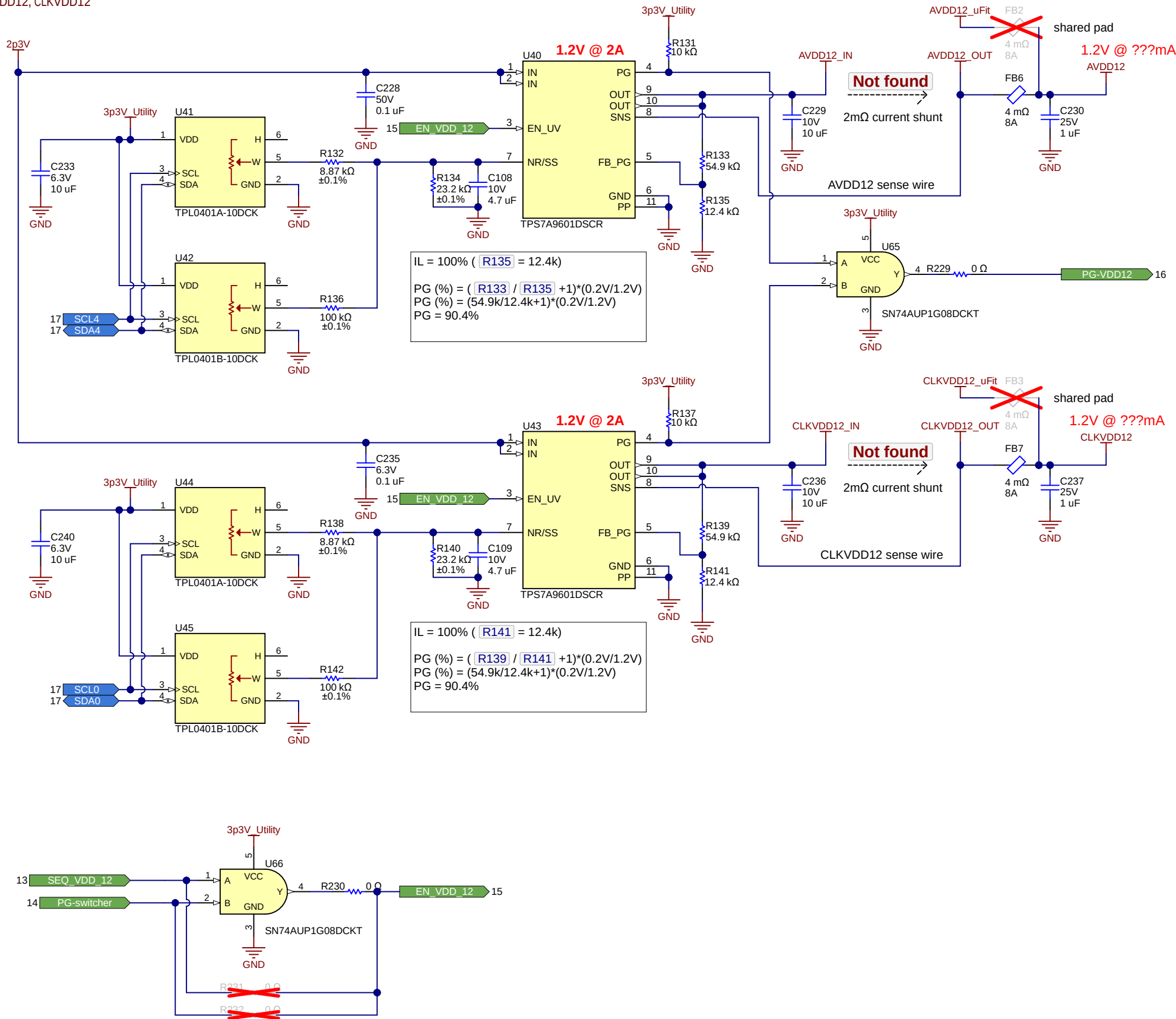


Single 12A mode
Switching Frequency = 2MHz
tss = 1ms
 $V_{out} = (36k\Omega / 20k\Omega) + 0.5V$
 $V_{out} = 2.3V$

This switcher feeds all 1.8V LDO and 1.2V LDO. It operates in 12A mode.

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EVM Power 3
AVDD12, CLKVDD12

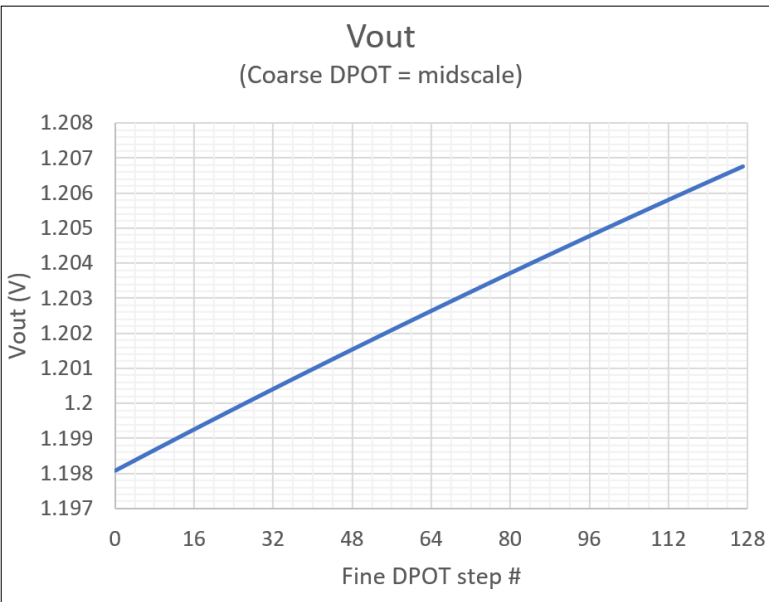
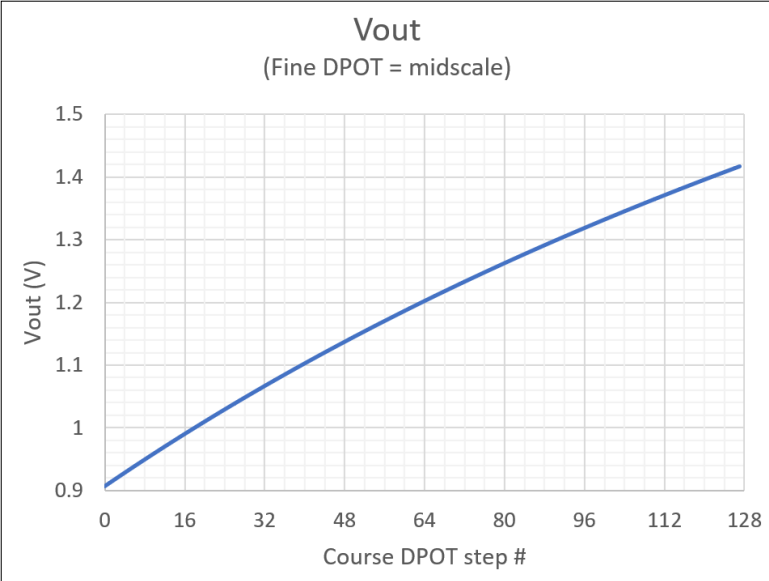


POWER UP SEQUENCE

1. DVDD (0.9V)
2. AVDD12 (1.2V) → CLKVDD12 (1.2V)
3. AVDD18 (1.8V) → CLKVDD18 (1.8V)

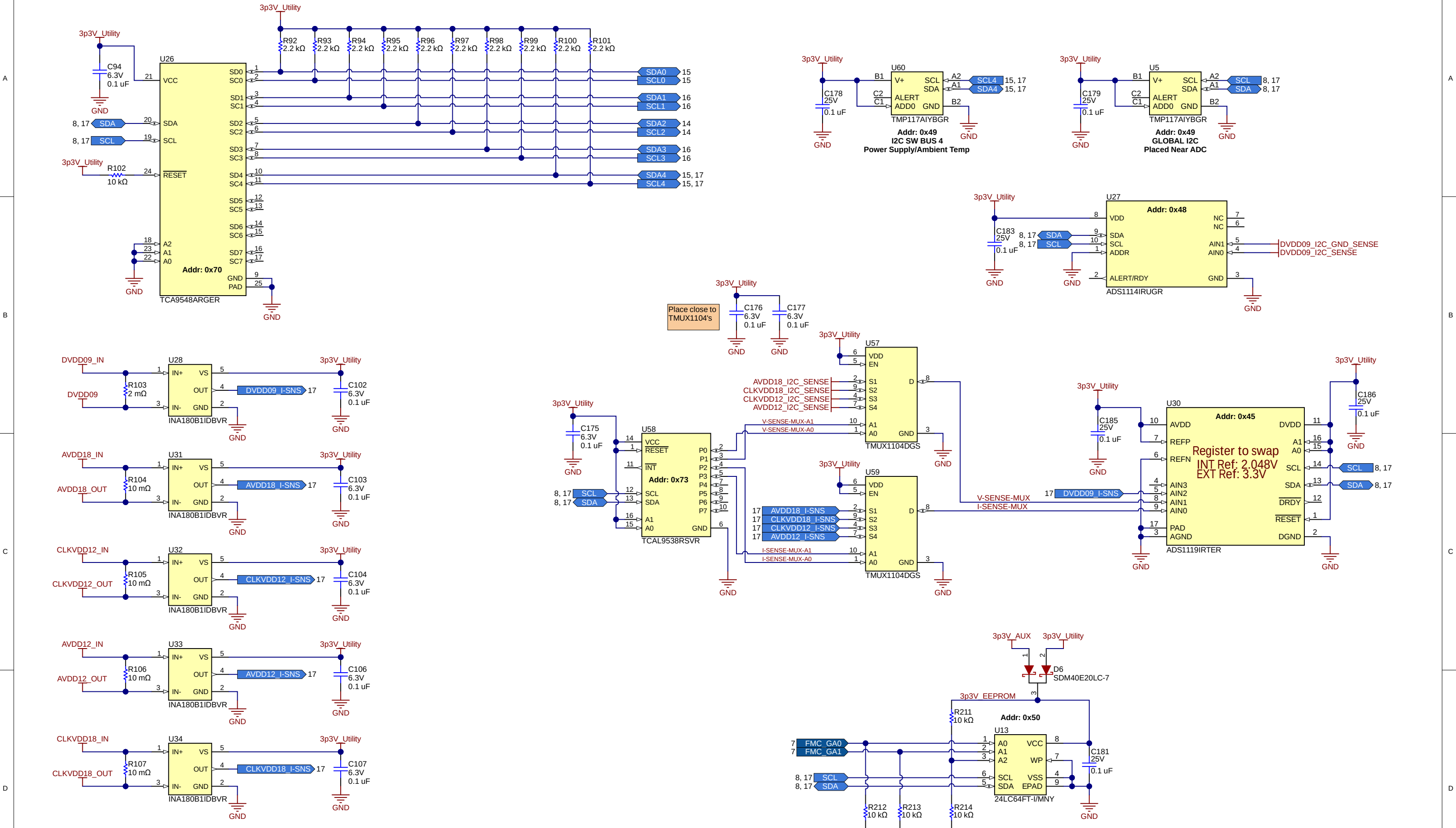
FOR ALL 1.2V MARGINING LDOs

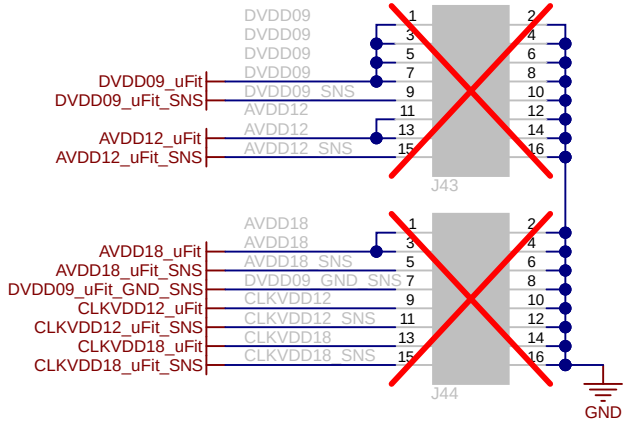
$$R_{NRSS} = 23.2k\Omega, R_{EQCOARSE}(nom) = 13.87k\Omega, R_{EQFINE}(nom) = 105k\Omega$$
$$R_{EQDPOTS}(nom) = \frac{13.87k\Omega * 105k\Omega}{13.87k\Omega + 105k\Omega} = 12.2516k\Omega$$
$$R_{EQDPOTS_{NRSS}}(nom) = \frac{12.2516k\Omega * 23.2k\Omega}{12.2516k\Omega + 23.2k\Omega} = 8.0176k\Omega \rightarrow V_{out} = 150\mu A * 8.0176k\Omega = 1.202V$$



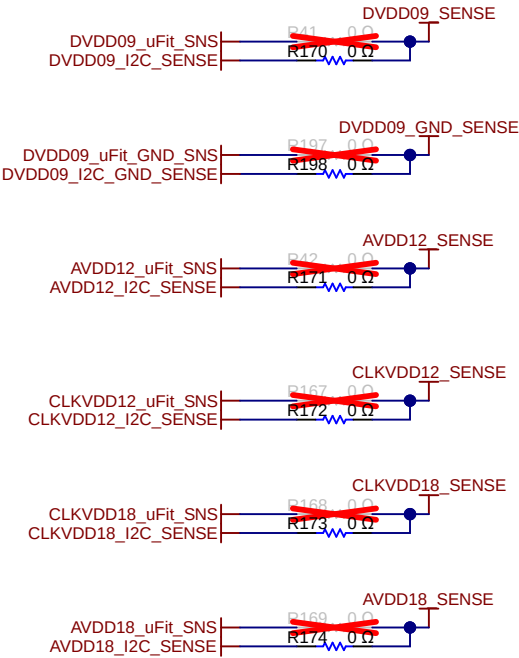
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I2C Devices





Place 0 ohm resistor close to existing sense line to leave minimal stub



Misc Hardware/Logos

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

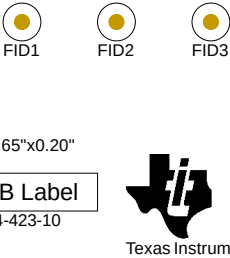
ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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Variant/Label Table	
Variant	Label Text
001	ADC3xRF7x_RevE2

Size: 0.65"x0.20"
LBL1
PCB Label
THT-14-423-10



PCB
LOGO
FCC disclaimer



PCB Number: -
PCB Rev: A



Orderable: Not For Public Release		Designed for: Not For Public Release		Mod. Date: 2/24/2025	
TID #: Not For Public Release		Project Title: ADC34RF7xEVM			
Number: -		Rev: A		Sheet Title: Misc Hardware/Logos	
SVN Rev: 3549342212367fc0980ad0322001e956605c042		ADC34RF75		Sheet: 19 of 19	
Drawn By: CW		File: ADC34RF7x_Misc_RevA.SchDoc		Size: B	
Engineer: CW		Contact: http://www.ti.com/support			

Rev History & Variants

Revision History

Rev	Release Date	Notes
E1	Jun. 14, 2024	Initial Release
E2	Aug. 09, 2024	• Swap GPIO3 and GPIO11 (fixes default SDO mapping) • Simplify SPI pullup/pulldown • Changes defaults for onboard power • Differential clock input (RF72 only) and single ended analog inputs • Fix LED current limit resistors • Swap AIN0 and AIN1 inputs on ADS1114 • Combines I2C buses with optional break point • I2C bus pullup decreased to 3.74kΩ • Added second TMP117 on I2C bus 4 near power supply • Replaced all INA226 with INA180 shunts • Uses I2C IO expander for switching supply sense MUXes • EEPROM uses low Vf diode for powering through 3p3V_UTILITY and 3p3V_AUX (if connected to supporting FMC) • Updated DNI list to remove uncommonly used headers which are in high density areas • SYNCb routed to H31 through shared pad
E3	Jan. 28, 2025	• Separates RESETb onto unique MUX for individual control • Allows break from RESETb to only use manual switch into watchdog • Adds 0Ω series R onto PDN and RESETb paths from FMC

Variant(s)

Variant	Notes
001	• ADC34RF72
002	• ADC32RF77

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